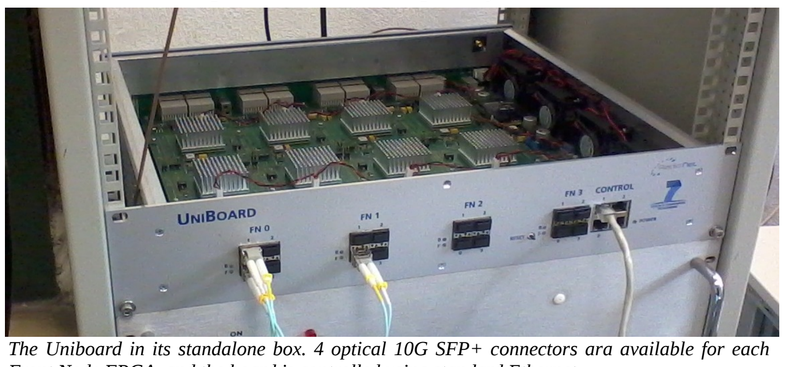
A 4 GHz digital receiver using the Uniboard platform

Giovanni Comoretto[a] , Antonietta Russo[a] , Benjamin Quertier[b] , Philippe Cais[b] and Pascal Camino[b]

a) INAF Osservatorio di Arcetri, Largo E. Fermi 5, Firenze, Italy;
b) Université de Bordeaux, Observatoire Aquitain des Sciences de l'Univers, 2 rue de l'Observatoire, BP 89, F-33271 Floirac Cedex, France;

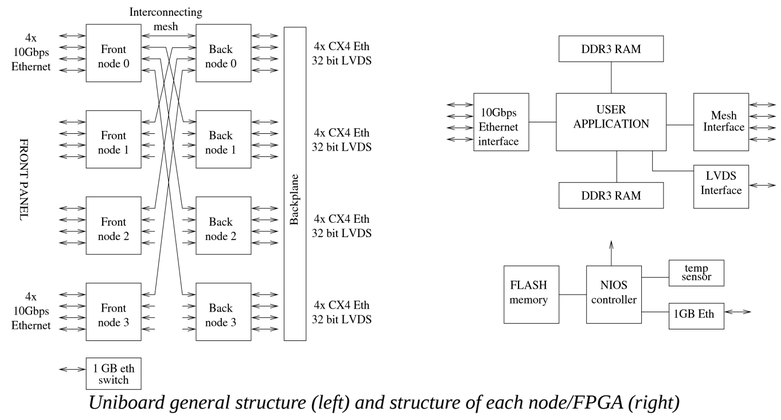
The Uniboard is a general purpose digital processing board, developed as a part of the Radionet FP7 program. It can be used standalone or as a part of a more complex system.



The Uniboard in its standalone box. 4 optical 10G SFP+ connectors ara available for each Front Node FPGA, and the board is controlled using standard Ethernet.

It is composed of 8 FPGAs, in two rows (back nodes, BN, and front nodes, FN) interconnected by a high speed mesh. Each FPGA has 4 10G Ethernet links, with optical SFP+ connectors on the front panel, and copper CX4 connectors on the backplane.

One or more ADCs can feed the board, using fast (800 MHZ) LVDS lines in the backplane.



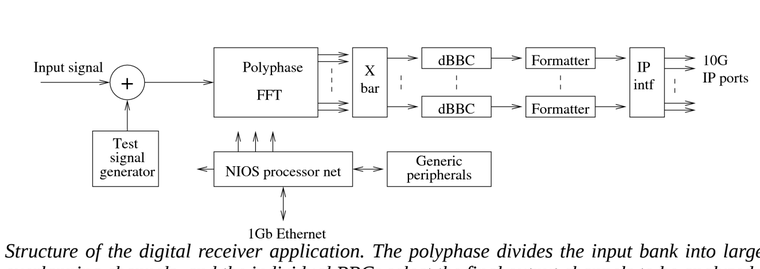
Uniboard general structure (left) and structure of each node/FPGA (right)

Each node contains a general controlling framework, based on the Altera NIOS soft processor, and a set of standard peripherals. The user application is seen as a set of programmable registers from the NIOS controller, and can be programmed using an internal 1G IP network and a custom UDP protocol.

The digital receiver application

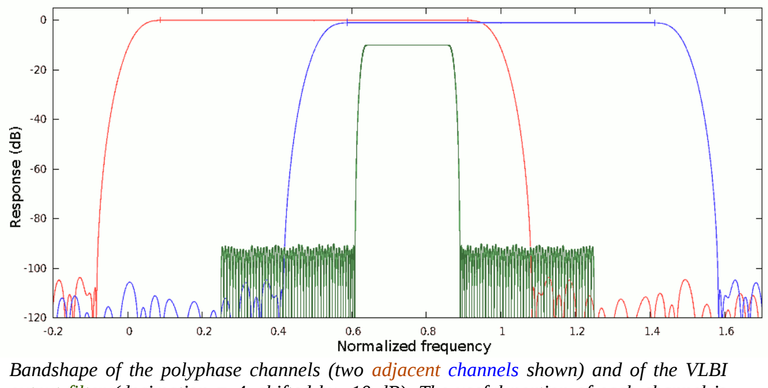
A Digital Receiver is a system composed of a fast ADC and a set of filters, local oscillators, and mixers that extract the portion of the input signal of interest, decomposes it into several narrow-band channels, and transmits them, in digital form, to the data analysis equipment. In the most extreme case the ADC directly analyzes the sky frequency, without intermediate frequency conversion stages.

The digital receiver developed for the Uniboard adopts a hybrid architecture: the input signal is first divided into equispaced overlapping bands by a polyphase filterbank. Then an array of digital baseband converters (BBC) select individual portions of each band. Each BBC has an independently programmable central frequency and bandwidth. The output of each BBC is then formatted and sent over one or more 10G IP ports.



Structure of the digital receiver application. The polyphase divides the input bank into large overlapping channels, and the individual BBCs select the final output channels to be analyzed

The input signal from 1 to 4 ADCs is fed to the Uniboard using the backplane LVDS ports. A test signal can be internally substituted to the input signal, and used for diagnostic purposes.



Bandshape of the polyphase channels (two adjacent channels shown) and of the VLBI output filter (decimation = 4, shifted by -10 dB). The useful portion of each channel is marked by ticks

Polyphase filter output bands have a nominal (Nyquist) bandwidth and sample rate that corresponds to the FPGA operating clock frequency. To avoid spectral holes between these bands, filter spacing is half the bandwidth, resulting in a nominal overlap of 50%. The actual overlap of the passband is lower, about 41% the nominal band. This allows full freedom for tuning an output channel of up to 1/4 the polyphase output sampling rate anywhere in the input band.

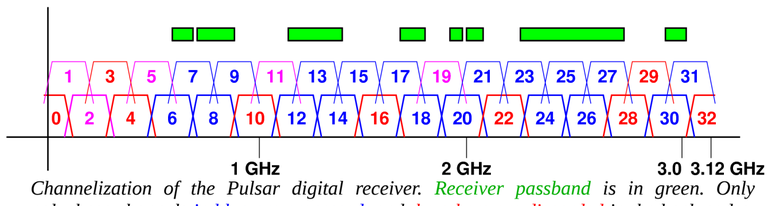
Specific applications

The above structure has been tailored for different applications:

Input band (GHz)	Output band (MHz)	N. of BBCs	Output format	Used resources
4	0.5-128	64	VDIF	BN+FN
2 x 2.0	0.5-128	64	VDIF	BN+FN
4 x 1.0	0.5-128	32	packet	BN
2 x 3.12	20	80+80	custom	BN+FN

The first three configurations are used for VLBI. The 4x1.0GHz configuration is implemented using only half board: the signal can be further processed (spectroscopy, RFI mitigation) in the front nodes.

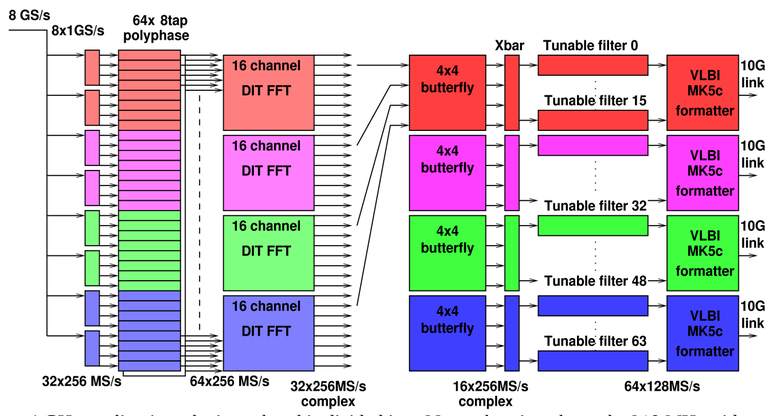
The last configuration is used in a wideband pulsar machine. The 3.12 GHz band in each polarization is divided into 32 overlapping channels of approx. 200 MHz each, spaced 100 MHz. Only a subset of these channels are processed, by 80 fixed band BBCs, allowing resource optimization and better RFI insulation. Due to the limited number of FPGA resources on the board, the BBC filter has an usable bandwidth of 82%.



Channelization of the Pulsar digital receiver. Receiver passband is in green. Only polyphase channels in blue are processed, and the others are discarded in the back nodes. Some channels are processed up to the polyphase FFT because the conjugate channel is used.

Implementation

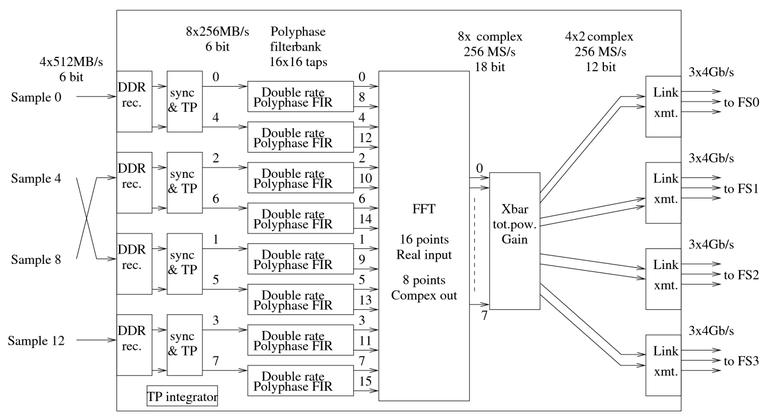
The system is physically distributed over the 8 FPGAs composing the board, except for the 1 GHz version that fits in a single back node per input channel. The 4 back node FPGAs implement the test signal generator, the filter section of the polyphase filterbank and the first 4 stages of the FFT, while the 4 front node FPGAs implement the last stages of the FFT, the DBBCs, and the formatter/IP layers.



4 GHz application: the input band is divided into 32 overlapping channels, 210 MHz wide and spaced by 128 MHz. A total of 64 BBC channels are available

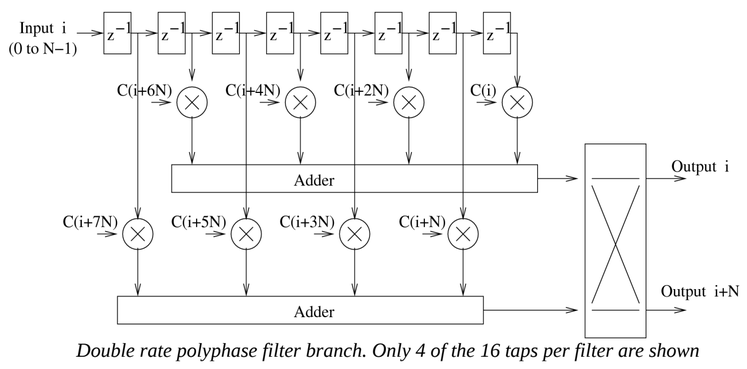
Polyphase filterbank

It is implemented in a distributed way among nodes.Each back node analyzes 1.0-1.6 GHz of interleaved input samples, and their outputs are combined in a final butterfly in the front nodes.



¼ of the polyphase filter (1 back node FPGA). Each parallel input sample is processed by the filter branch below. Only lower half of the outputs are forwarded to the front nodes

Each parallel input sample is processed in a double rate polyphase filter branch, that computes inputs *i* and *i+N*. Outputs are interchanged at each clock cycle, to remove frequency reversal on odd FFT channels.

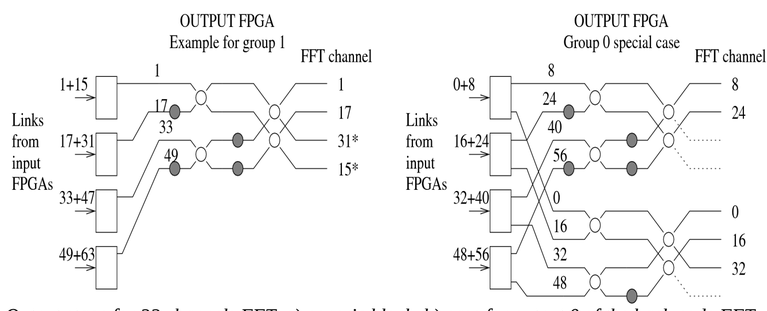


Double rate polyphase filter branch. Only 4 of the 16 taps per filter are shown

Final stages of the FFT are implemented on the front nodes, with each FN processing two BN outputs. To optimize communication between back and front nodes, only first half of the back node FFT are transmitted, as the other half can be derived by complex conjugation. Signals are requantized to 8-12 bit to reduce the data flow. This reduces the channel-to-channel insulation. Actual insulation for noiselike Gaussian signal has been derived from simulation

N. bits (BN->FN)	Insulation (dB)
8	70
9	76
12	95

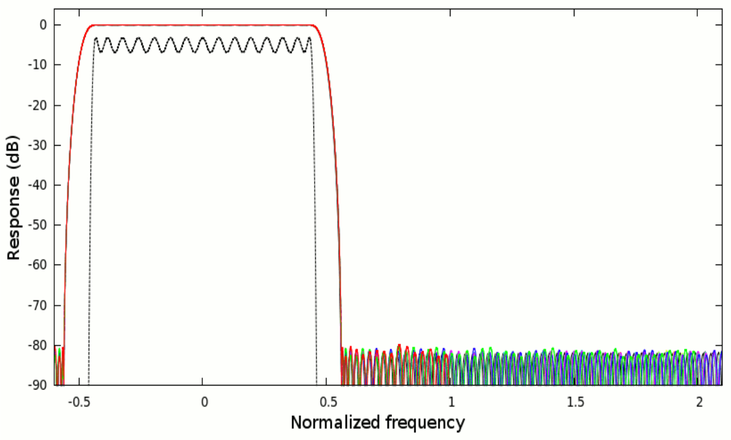
The final stage exploits the complex conjugate relationship among back node signals and FFT outputs to reduce the number of multipliers used:



Output stage for 32 channels FFT. a) generic block, b) case for output 0 of the back node FFT.

Digital baseband converter

Each polyphase channel is analyzed by a set of tunable baseband converters. Final band corresponds to ½ to 1/256 the input band (the pulsar version has a fixed decimation rate of 1/8), and the output can be either real or complex. Useful flat bandwidth is 88% and 82% for VLBI and pulsar configurations, resp., independently on decimation. Stopband attenuation is > 80 dB. Filter coefficients have been computed by extending the FIR response of the smaller filters by interpolation, and then optimizing some critical regions of the FIR response.



Passband of the BBC filters, for decimation between 2 and 256, normalized to the output sampling rate. Dashed curve is the passband magnified by 1000 times to show its ripple

Final formatting

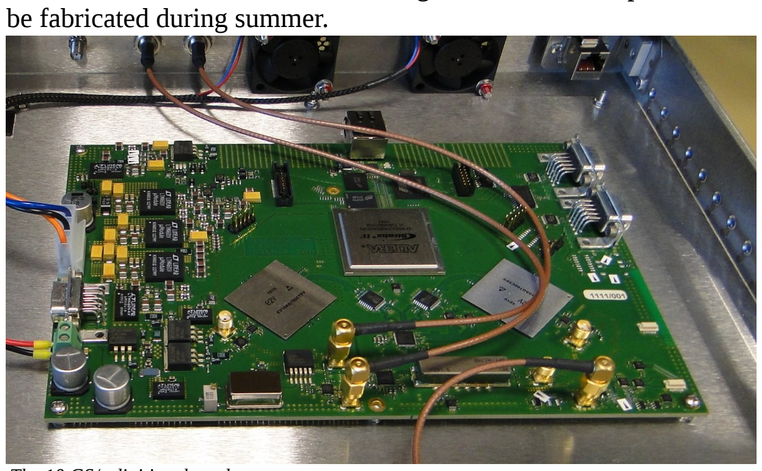
The BBC outputs are formatted in packets of approx. 8Kbytes each (IP Jumbo frame), in a standard UDP packet. Destination port and IP address is selectable for each packet, to implement distributed correlation. Packets with different destinations can be sent over the same physical link.

The VLBI receiver uses VDIF format. Each BBC uses a separate VDIF stream. The pulsar receiver outputs a total of 1.6 GHz in double polarization, over 12 10G links. Each link carries up to 8 double polarization BBC channels, for a total of 320 MHz (640 MS/s @8 bits)

ADC modules

The pulsar version uses two 6.4Gs/s commercial ADCs. For the VLBI version, a 6 bit 8GS/s ADC is being developed at UdB. At the moment, a 10 GS/s (but with analog band of only 3 GHz) has been built for testing.

A 8GS/s 3 bits full custom ASIC digitizer, on 65 um process, will be fabricated during summer.



The 10 GS/s digitizer board