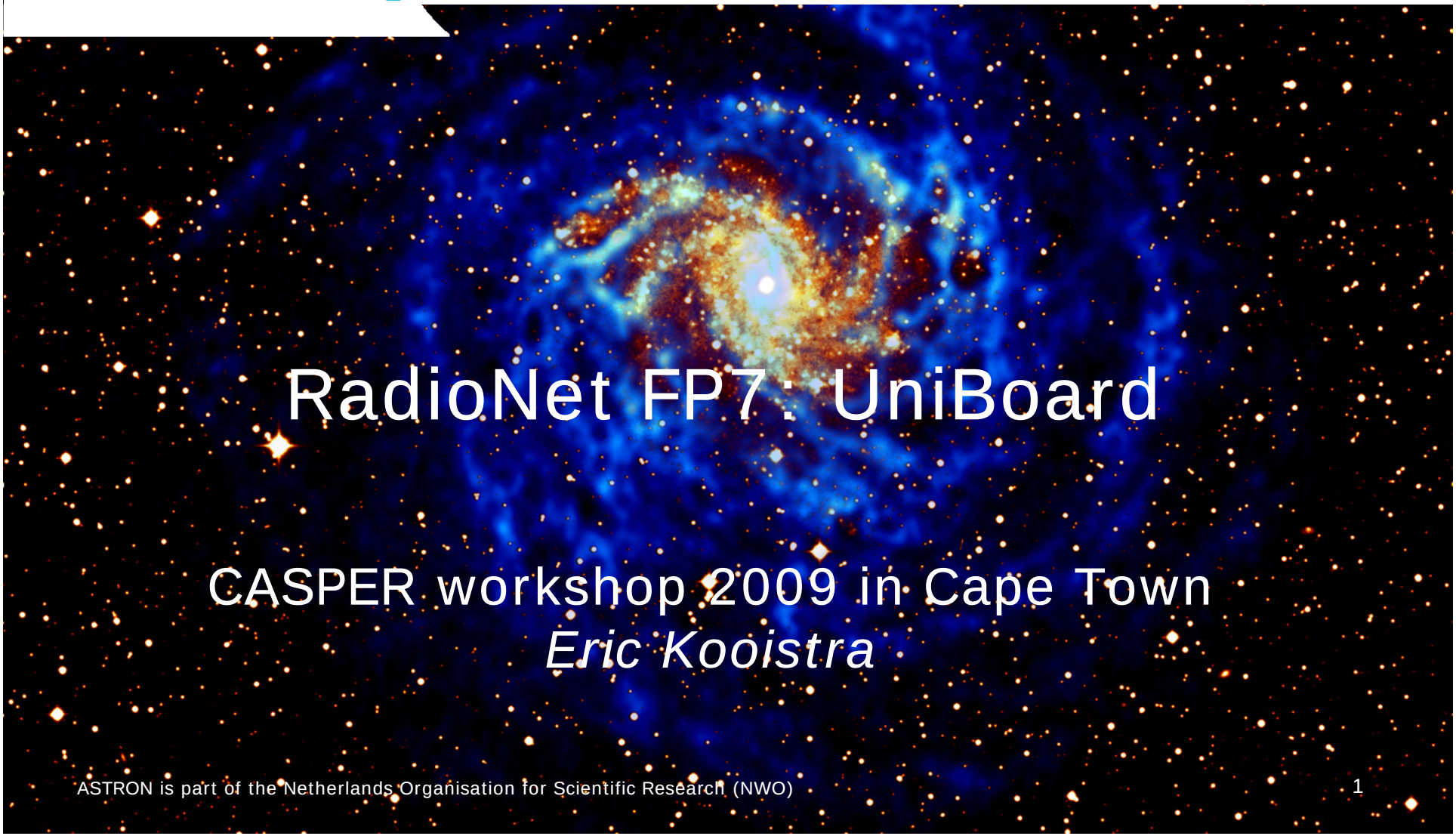
ASTRON

Netherlands Institute for Radio Astronomy



RadioNet FP7: UniBoard

CASPER workshop 2009 in Cape Town

Eric Kooistra

Contents

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RadioNet FP7

- European program for radio astronomy
  - 26 partners, coordinator Mike Garrett (ASTRON)
  - 10 M€ over 3 years
  - Started Jan 2009
- Several joint Research Activities one of which is UniBoard

Contract no. 227290

The RadioNET FP7 UniBoard Research Activity

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- The project lead is by Arpad Szomoru (JIVE)
- UniBoard is a generic digital board for Radio Astronomy applications:
  - FX, BF, Digital receiver, Pulsar machine, RFI mitigation
- The board design is done by ASTRON (lead by Andre Gunst)
- The test firmware development is done together by ASTRON/ JIVE
- The application development is done by the partners:
  - Netherlands : ASTRON, JIVE
  - France: Bordeaux University, University of Orleans
  - Italy : INAF
  - UK : University of Manchester
  - Korea : KASI

From LOFAR Technology to UniBoard

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- LOFAR is the Low Frequency Phased Array Radio Synthesis Telescope built by ASTRON
- The digital processing in the LOFAR antenna stations is done in subracks equiped with two kinds of processing boards:
  - RSP boards for filtering, beam forming and calibration:
    - 5 Virtex4 FPGAs, 12 or 24 boards per station
  - TBB boards for transient data capturing
    - 5 Virtex4 FPGAs + 8 GByte DDR2 memory, 6 or 12 boards per station
- The photos on next slides quickly zoom in to the digital processing boards starting at the LOFAR core.


Skagerrak
Göteborg
Kattegat
Baltic Sea
Denmark
København
(Copenhagen)
Malmö
North Sea
Sylt
Amrum
Douglas
Irish Sea
Dublin
Juist
United Kingdom
Berlin
Amsterdam
Netherlands
Bristol Channel
London
Germany
Bruxelles
Brussel
(Prague)
Praha
Czech Republic
English Channel
St Peter Port
Jersey
Luxembourg
Luxembourg
Paris
(Vienna)
Austria
© 2009 Google
© 2009 Europa Technologies
© 2009 Tele Atlas
© 2009 Basarsoft
Liechtenstein
Bern
46°02'21.45" N
16°31'17.91" E
elev 1134 ft
Eye alt


Spiekeroog
Langeoog
Norderney
Mellum
Memmert
Borkum
Amsterdam
Overijssel
Netherlands
Image © 2009 GeoContent
© 2009 Europa Technologies
© 2009 Tele Atlas
Image © 2009 Aerodata International Surveys
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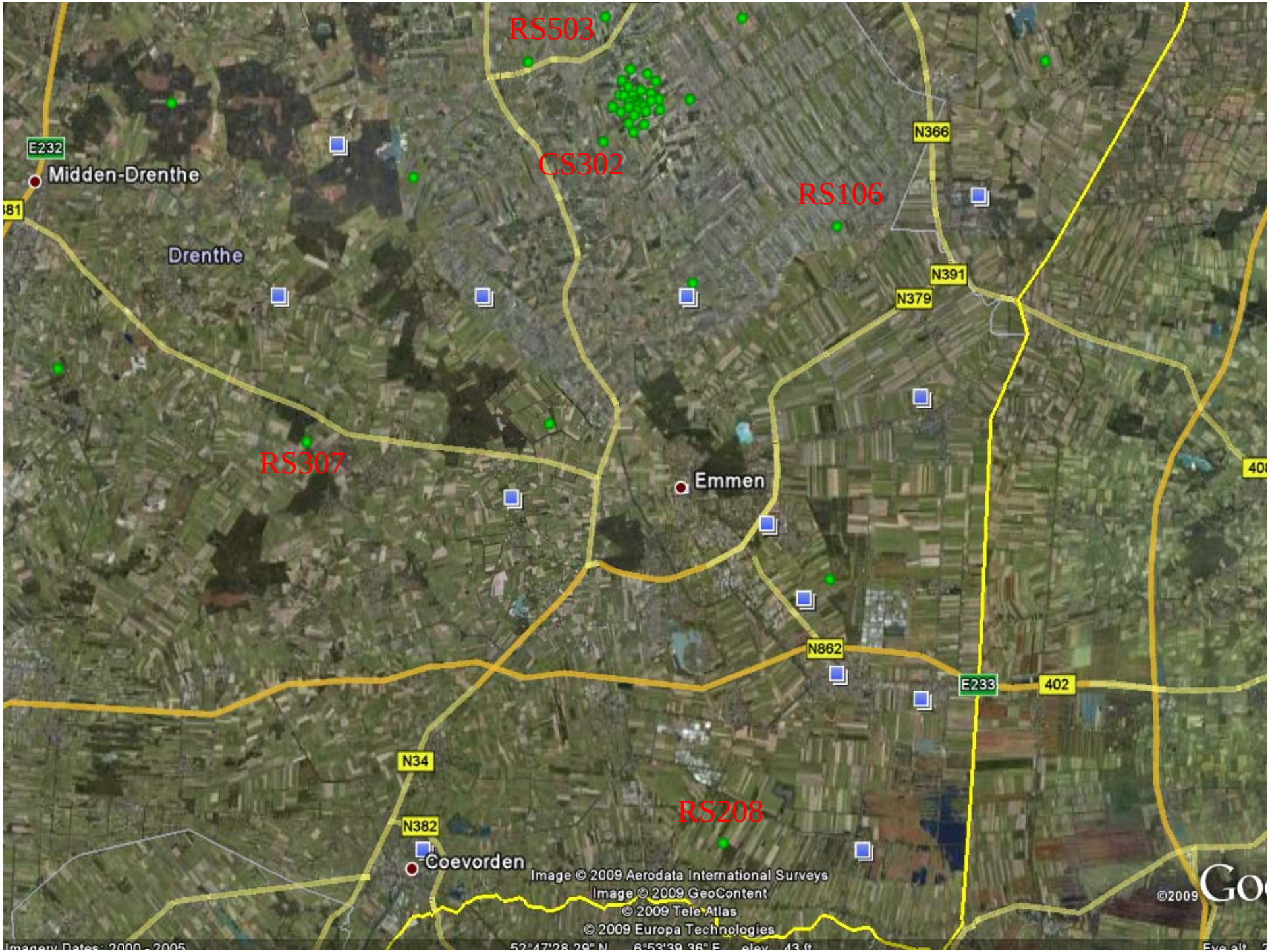
RS503
CS302
RS106
RS307
RS208
E232
Midden-Drenthe
Drenthe
N366
N391
N379
Emmen
N862
E233
402
N34
N382
Coevorden
Image © 2009 Aerodata International Surveys
Image © 2009 GeoContent
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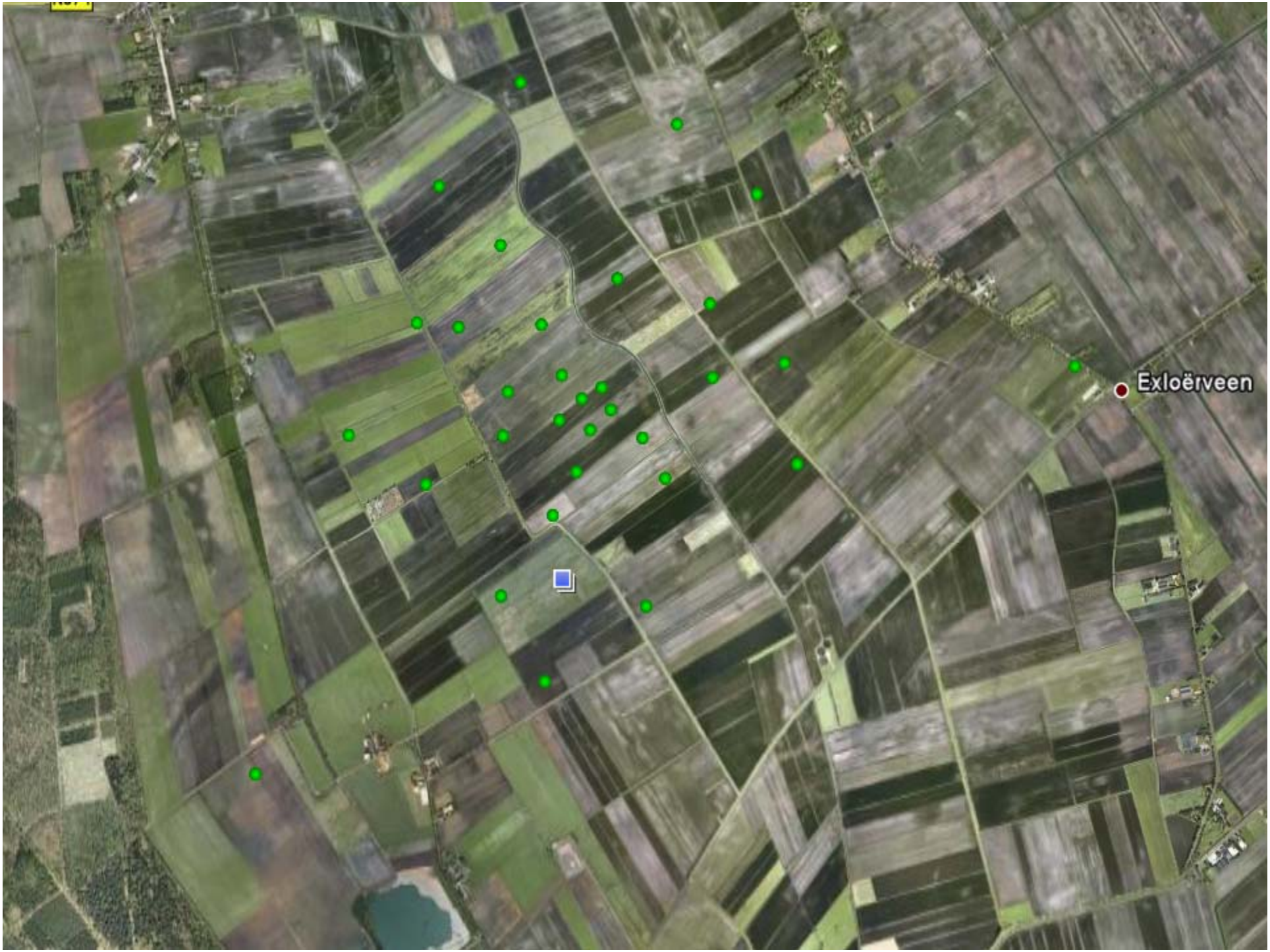
Exloërveen


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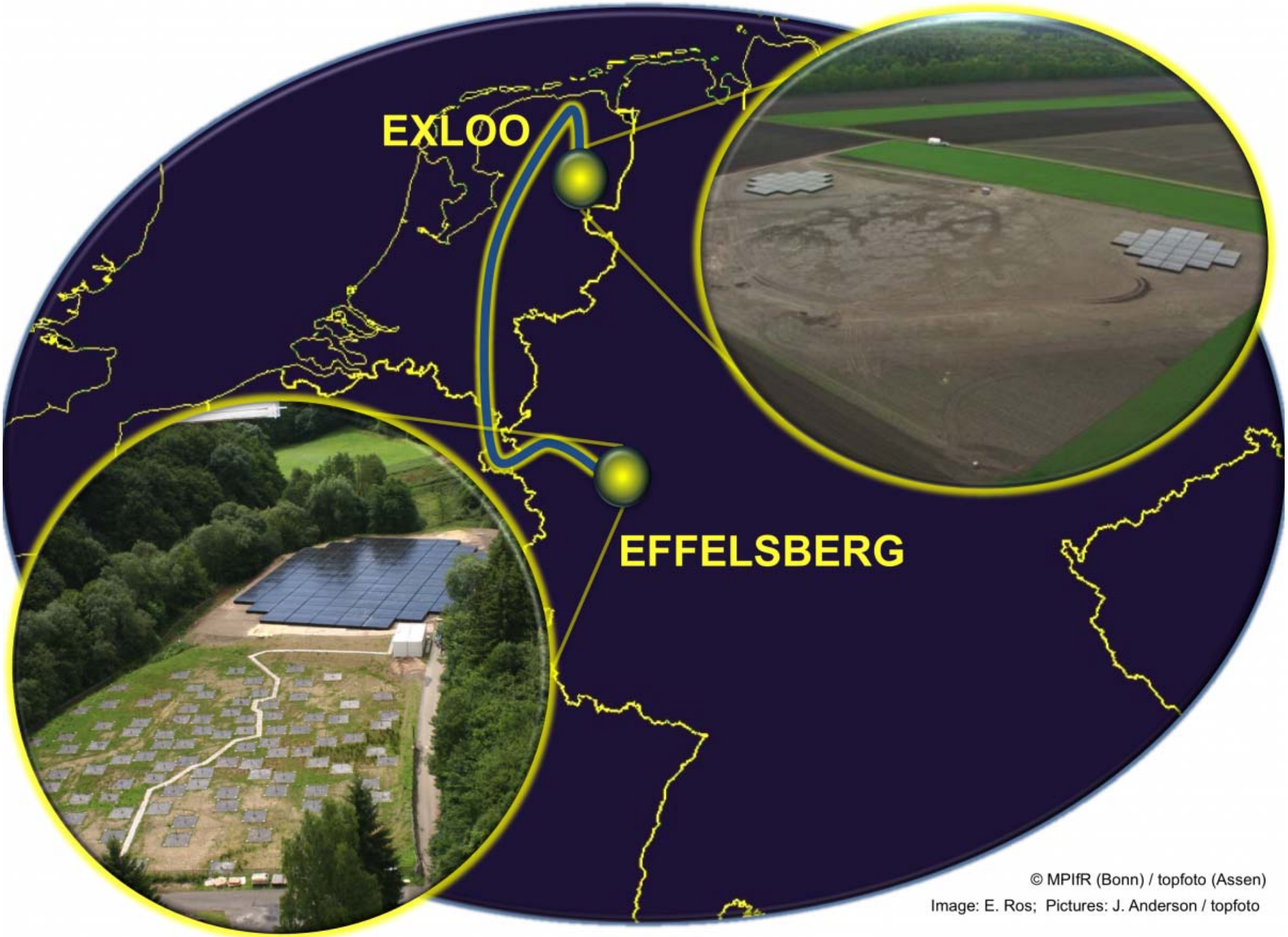

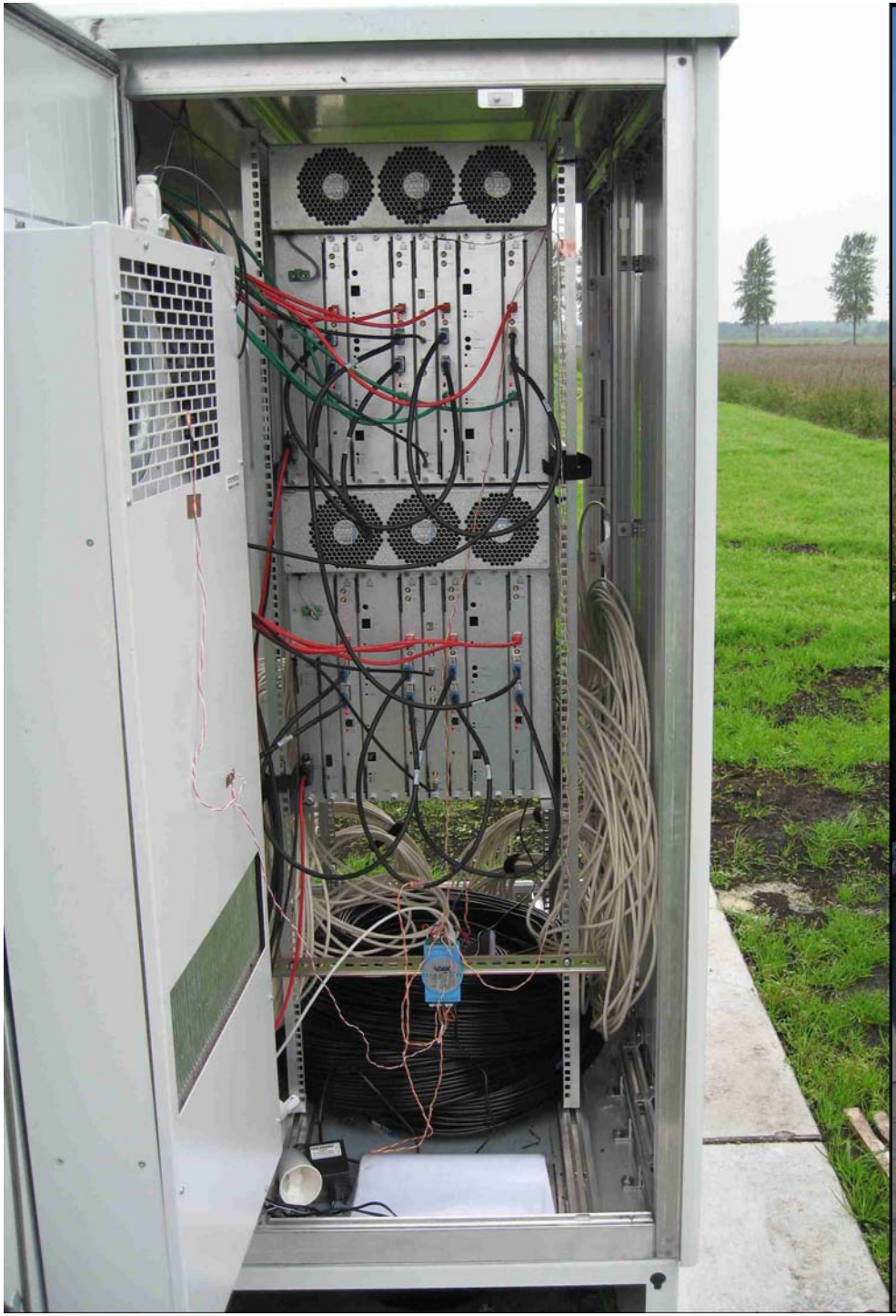

Station Digital Processing Board

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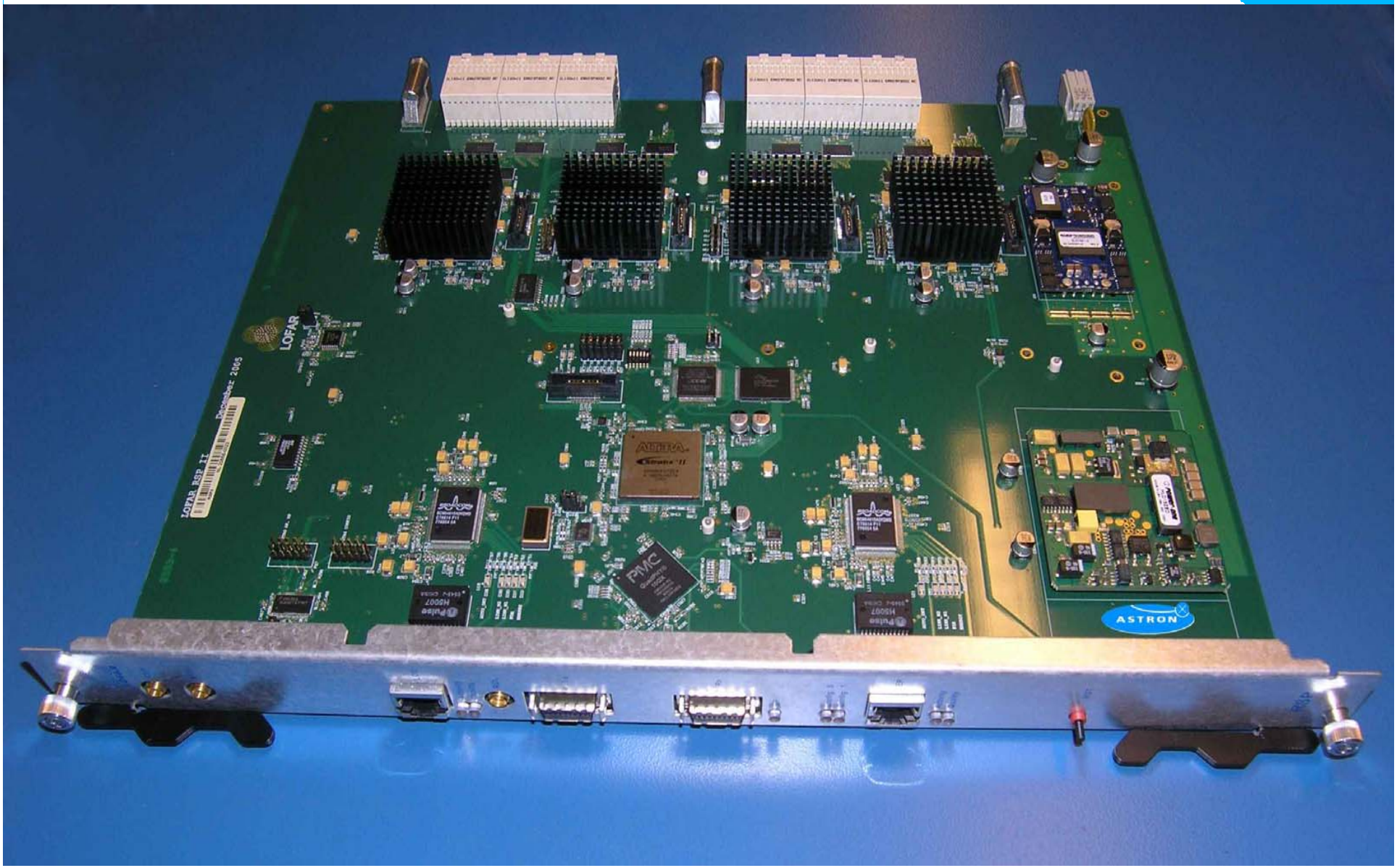

Transient Data Buffering Board

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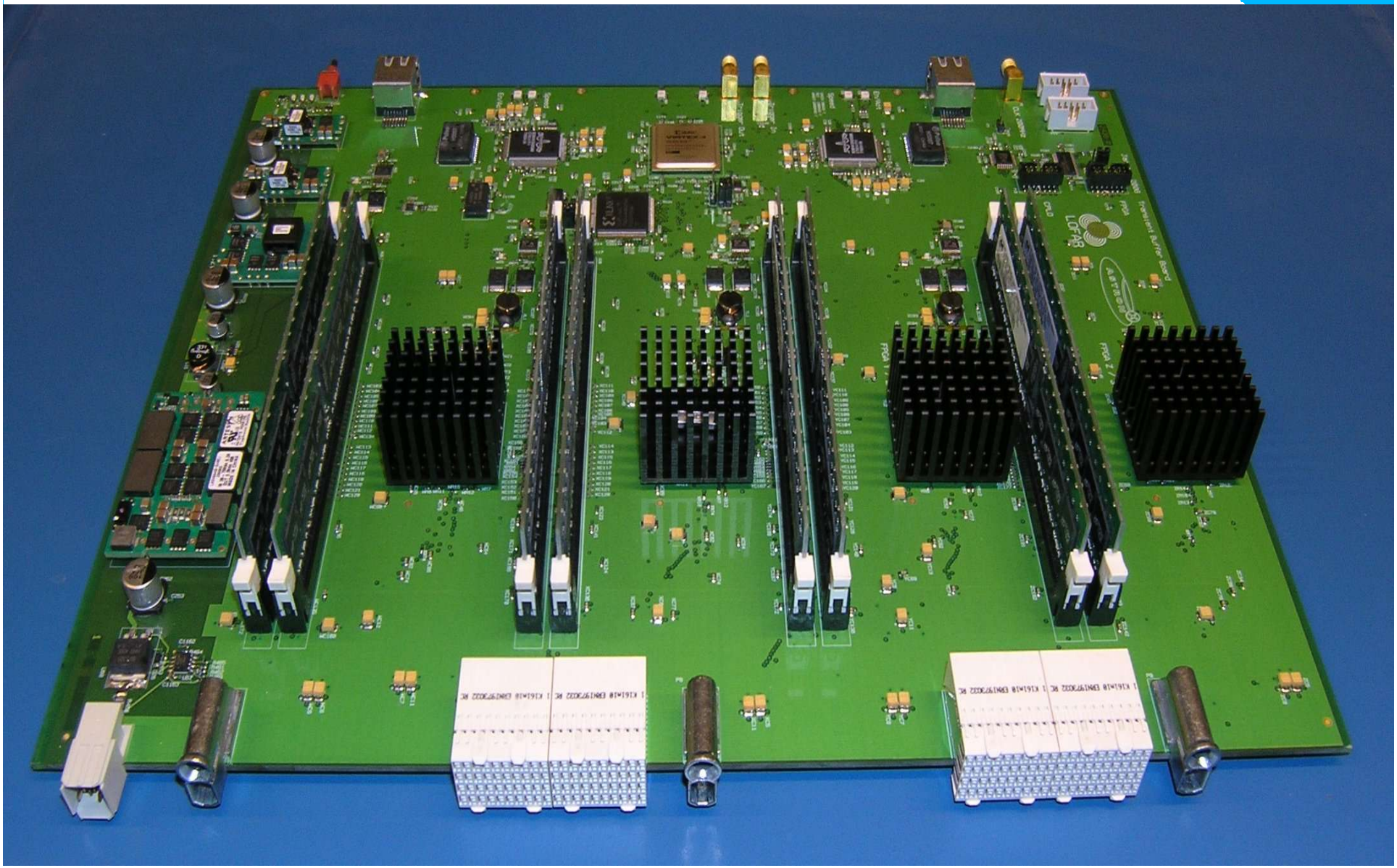

UniBoard Philosophy

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- Continue on the approach we had for LOFAR:
  - High integration density
  - Scalable allowing one, more or many boards
- Use 10GbE interfaces for data IO
- All FPGAs should have the same capabilities
- Usage of one type of board for multiple applications
- The firmware makes the board application specific
- Model Based Design for more rapid application development

Types of Processing Targeted for UniBoard

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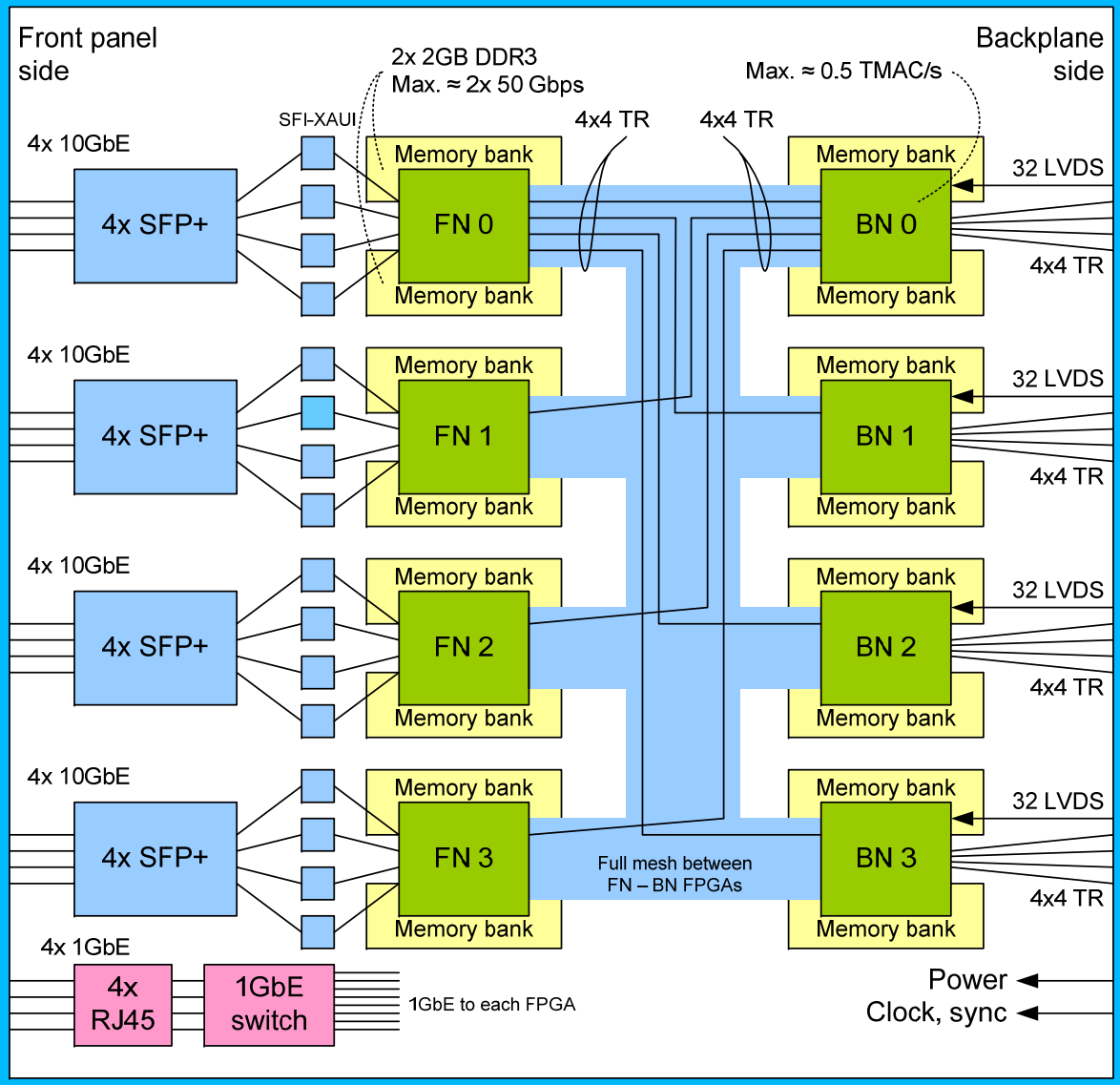
- Input processing
  - Filterbank
  - Digital receiver
- Output processing
  - Beamformer
  - Correlator (FX)
  - Pulsar processing
- Architecture uses the independency of:
  - Subbands (different frequencies)
  - Beams (different directions)

UniBoard Block Diagram



Why Altera Stratix IV for UniBoard?

ASTRON

- Xilinx and Altera FPGAs are comparable in technology and tools
- We want 40 nm process for low power and newest technology
- In 40 nm Altera offers Stratix IV and Xilinx offers Virtex 6, but only the Altera EP4SGX230KF40 is available mid 2009
- The EP4SGX230KF40 fits the needs for UniBoard and at a feasible price so that is why we chose it

- For comparison: the EP4SGX230KF40 features somewhere between the Xilinx Virtex 6 LX240T and the Virtex 6 SX315T

UniBoard Power Consumption Estimate

ASTRON

	Power each	Number	Total
FPGA	20 W	8	160 W
Interfaces (10GbE)	2 W	16	32 W
Memory (DDR3)	2.5 W	16	40 W
Power supply	loss 20%	1	46 W
Total power			280 W

Extending Uniboard to a System

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- With N nodes each node processes 1/N part of the total processing.
- Minimize number of hops:
  - Full mesh between front nodes and back nodes on UniBoard
  - Full mesh beteen corresponding back nodes on backplane
- With 16 transceivers per back node FPGA there can be up to maximum 9 UniBoards in a subrack.
- No need for 10GbE switches to interconnect FPGAs.

UniBoard and 10GbE switches

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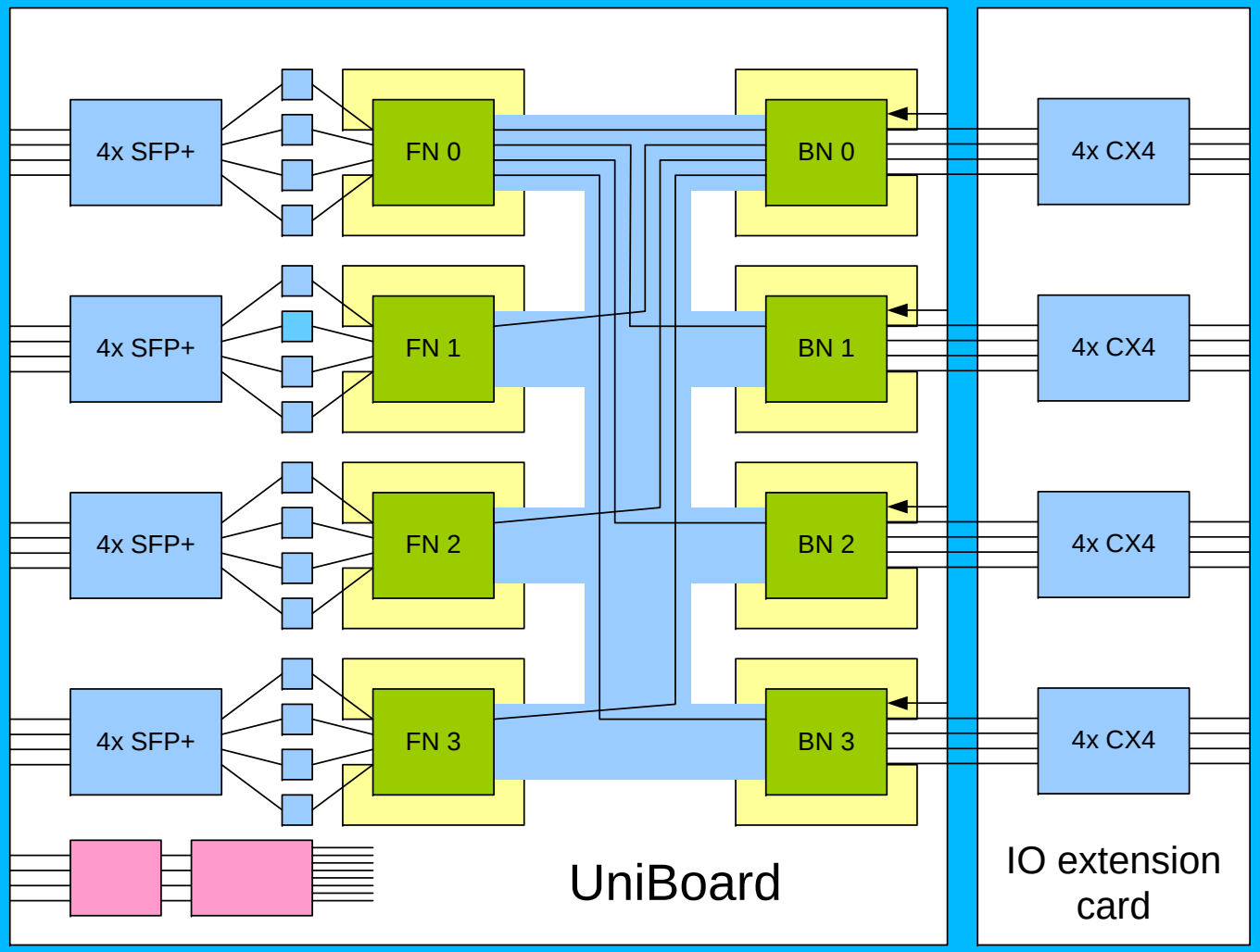
- 10GbE switches are not for free: 7 W/port, $600 /port.
- With 2-4 10GbE ports per FPGA the cost of switches becomes comparable to the cost of FPGAs.
- For user IO we may need to use 10GbE switches to rearrange data streams.
- Using a 10GbE IO extension card at the back of the UniBoard still allows replacing the backplane by 10GbE interconnect via 10GbE switches.

UniBoard with 10GbE IO Extension Card



Main Applications Driving the UniBoard

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The main performance requirements regarding IO, processing and memory come from:

- EVN2015 correlator (JIVE)
- APERTIF beamformer (ASTRON)
- APERTIF correlator (ASTRON)

EVN2015 Correlator

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UniBoard for EVN2015 Correlator

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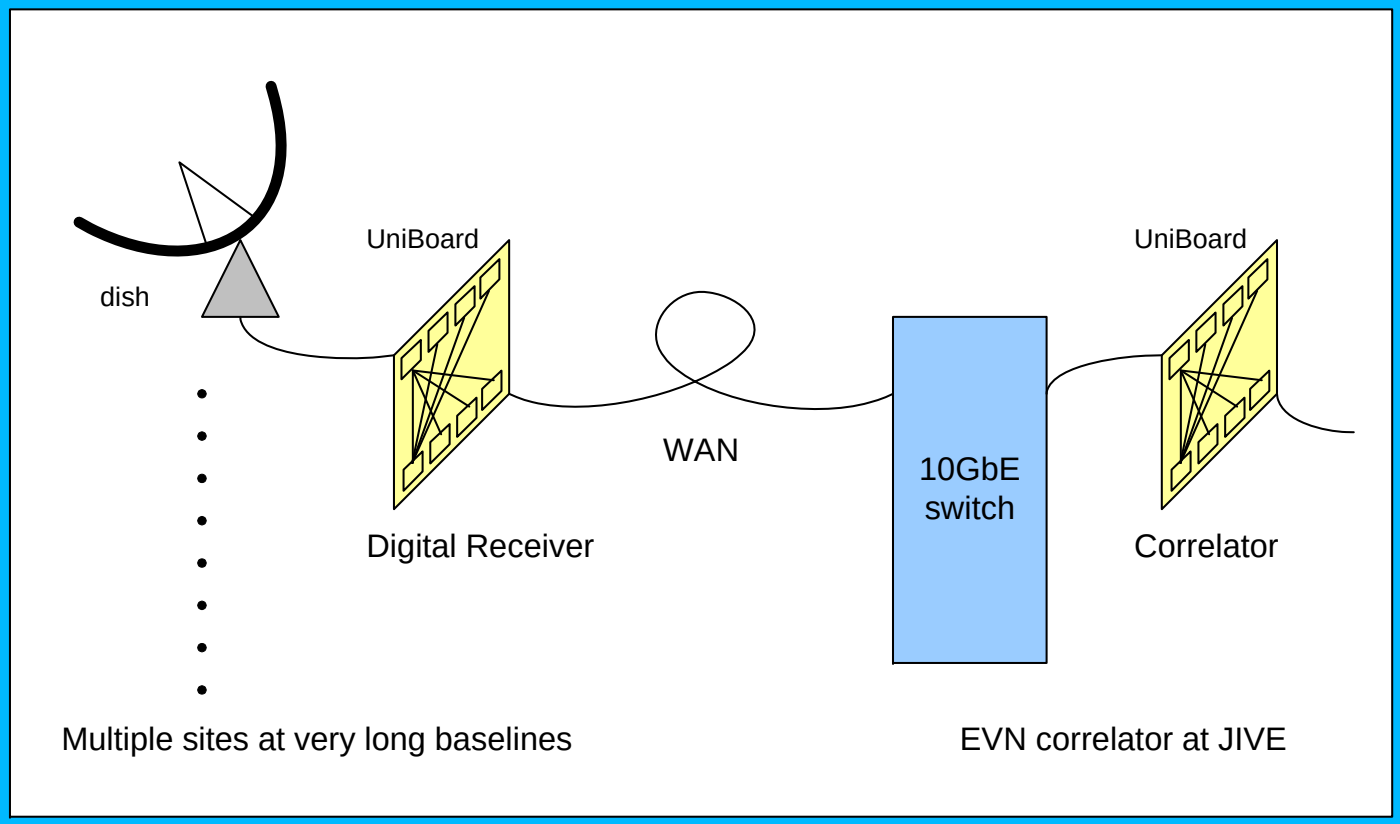
- 32 dual polarization antennas, so 2080 visibilities
- 2 GHz RF input bandwidth



APERTIF Focal Plane Array at WSRT

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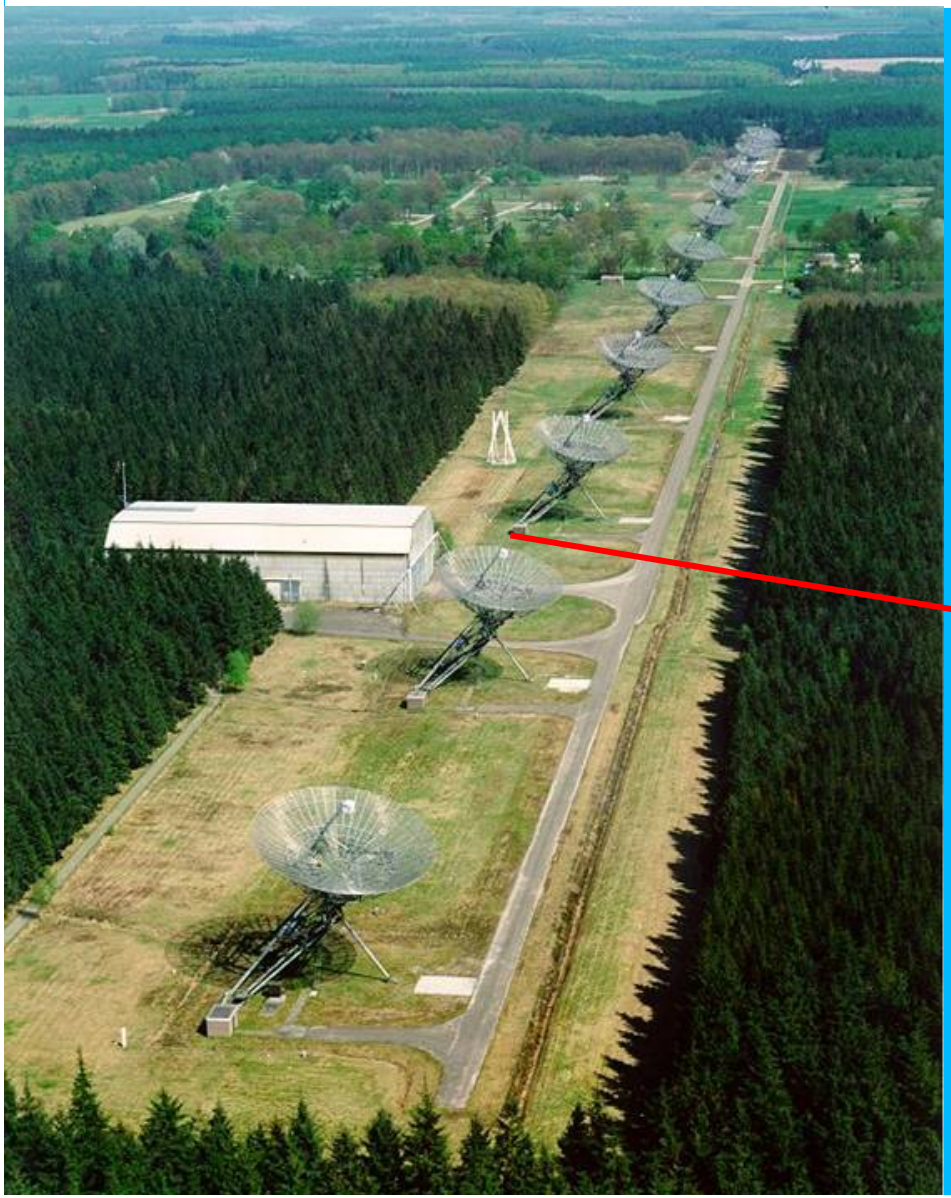

APERTIF Requirements

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- Beam former:
  - 12 Westerbork 25 m dishes each with a Focal Plane Array
  - 60 dual polarization antennas per telescope
  - 400 MHz RF input bandwidth
  - 300 MHz beam output bandwidth
  - 37 beams

- Correlator:
  - 12 dual polarization FPA telescopes
  - 37 beams, so in total 11000 visibilities

UniBoard for APERTIF Beamformer

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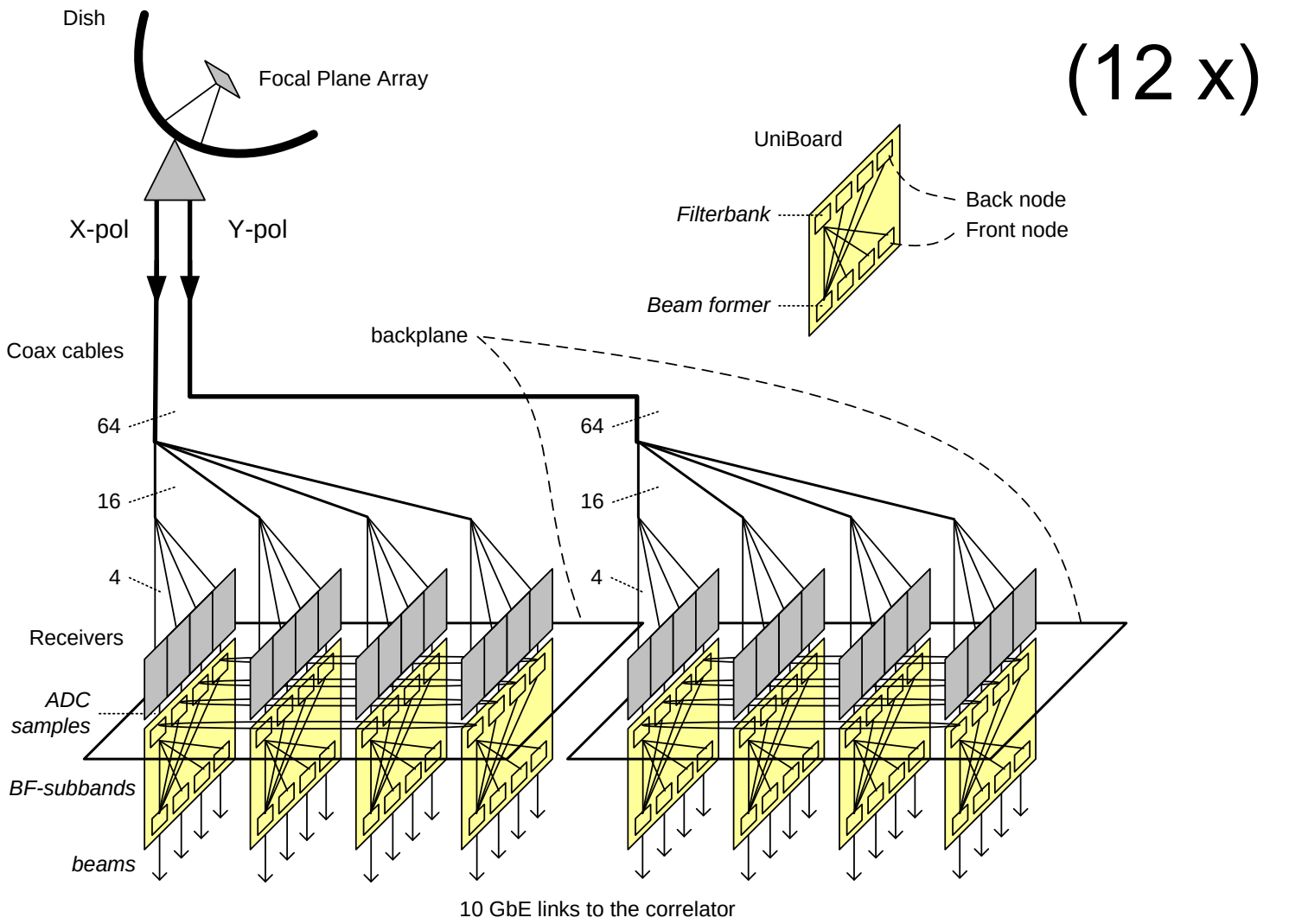

UniBoard for APERTIF Correlator

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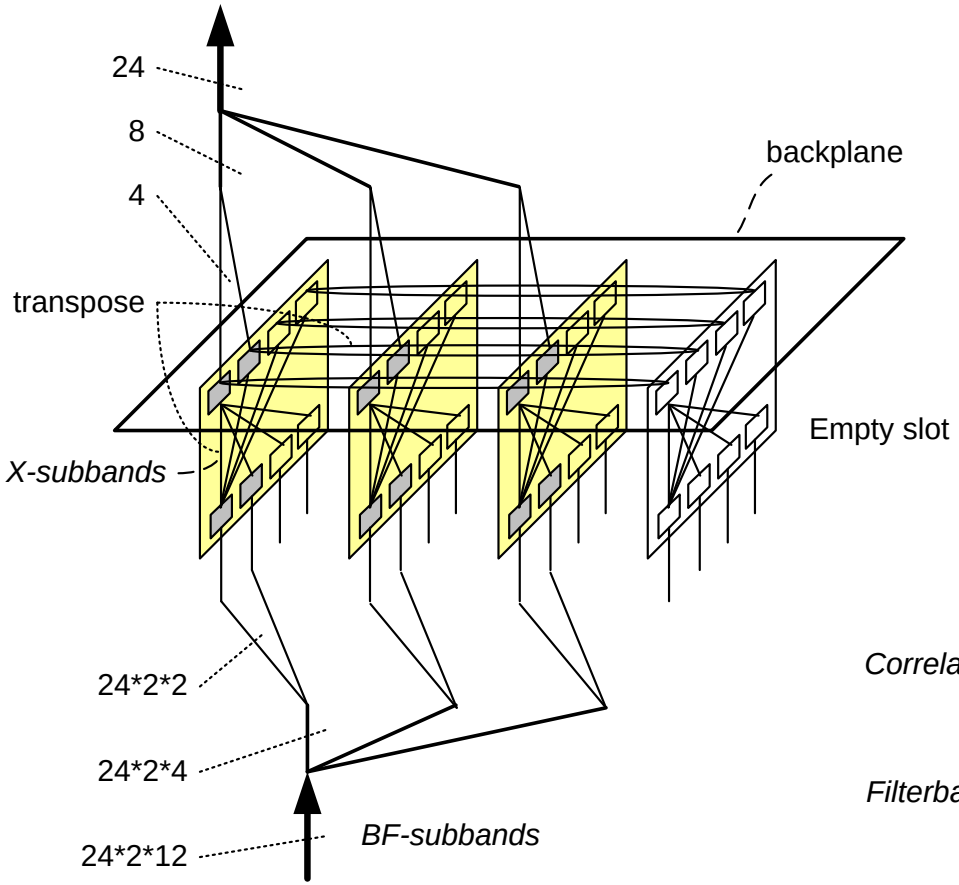
Full Stokes visibilities of 24 BF-subbands bandwidth and for all beams to the post processing via 1 GbE control links



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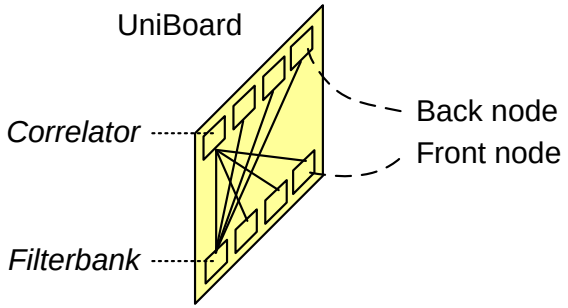

All beams with each 24 dual pol BF-subbands from 12 telescopes

UniBoard for APERTIF Summary

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Processing	Processing [TMAC/s]	Nof UniBoards (FPGAs)	Utilization GMAC/s/FPGA
APERTIF BF	94	96 (768)	122 (24%)
APERTIF X	25	24 (192)	130 (25%)

IO	Data rate [Tbps]	Nof 10GbE (front FPGAs)	Utilization Gbps
APERTIF BF	Out: 2.1	384 (384)	5.5 (55%)
APERTIF X	In: 2.1	384 (96)	5.5 (55%)

UniBoard Firmware Development Plan

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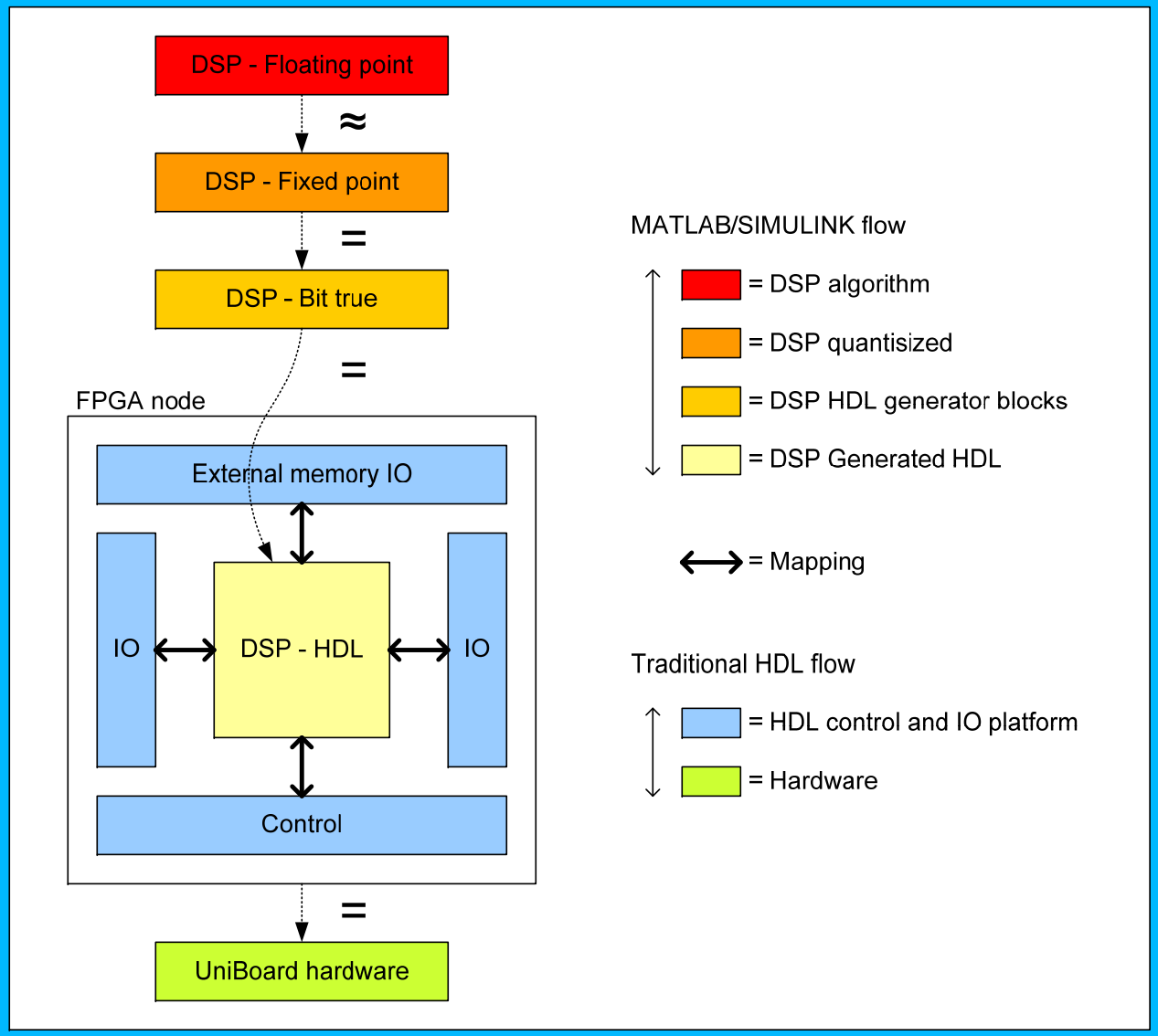
1. Test Firmware:
   - Verify the FPGA pin assignments
   - Verify all hardware interfaces of the Uniboard

2. Application Firmware:
   - Provide a HDL control and IO platform
   - DSP functionality for an astronomical application
   - Towards Model Based Design

Concept Model Based Design Flow



UniBoard Status

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- Schematic design finished and reviewed
- Board manufacturer selected
- Board layout 50% done
- Test firmware writing ongoing
- Model Based Design started

UniBoard Layout ongoing

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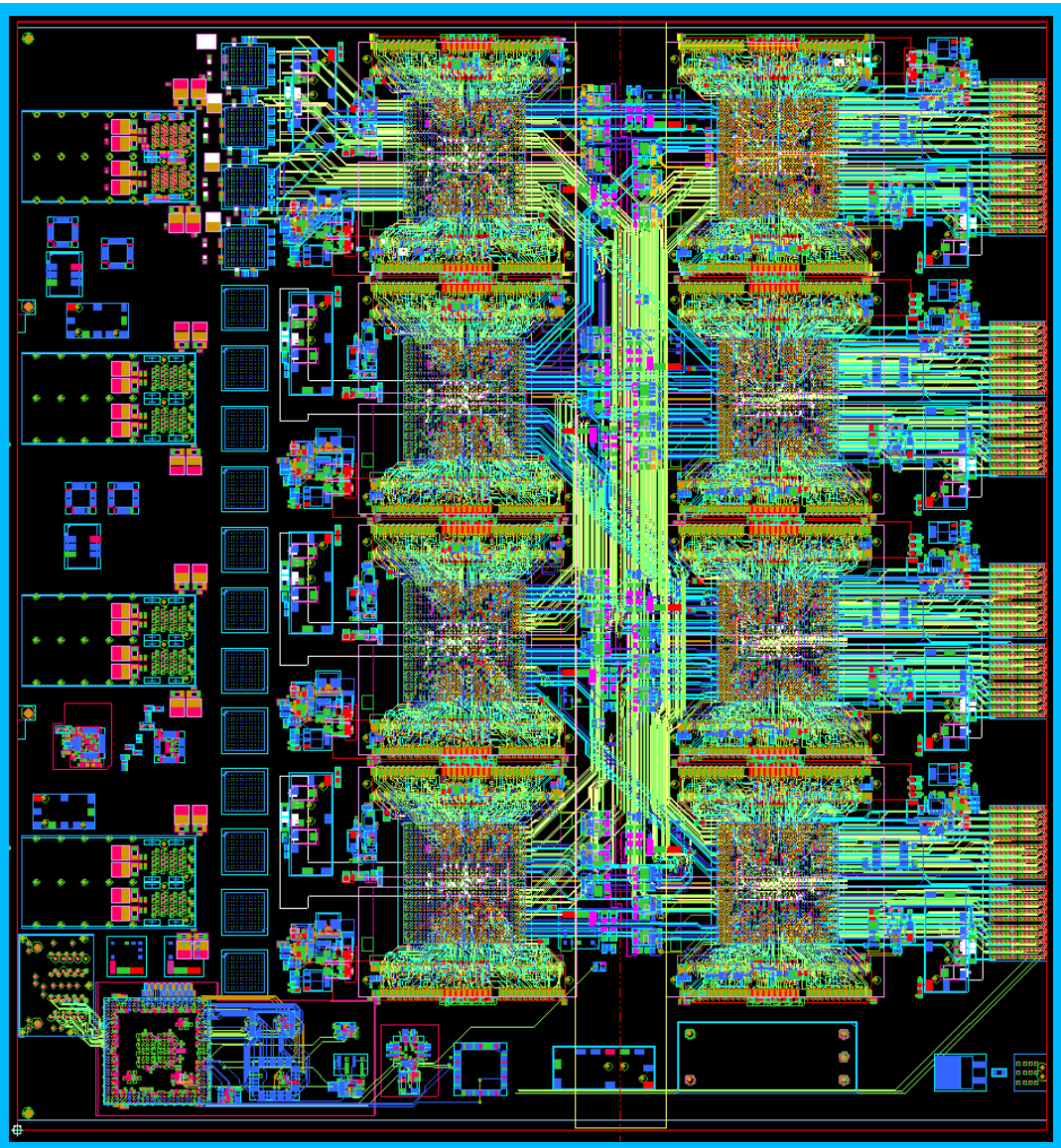

- H x D x T =
  9HE x 340 x 2.4mm
- 12 layers PCB

UniBoard Planning

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- End 2009 : First UniBoard in production
- Mid 2010 : First UniBoard fully tested, subrack in house
- End 2010 : Second UniBoard in house, subrack tested
- Mid 2011 : Second UniBoard fully tested
- End 2011 : System tests done

UniBoard Conclusion

ASTRON

- Integrated solution using multiple FPGAs per board, multiple boards in a subrack (continue on LOFAR experience)
- Per UniBoard 4 front node FPGAs and 4 back node FPGAs:
  - 8 x two DDR3 memory banks
  - 4 x four 10GbE links at the front
  - 4 x 16 transceiver links at the back
  - 4 x 32 bit LVDS inputs at the back to connect ADCs
- Up to 9 UniBoards in a subrack (application dependent)
- Uses Stratix IV 40nm FPGA (EP4SGX230KF40)
- One type of board suitable for multiple applications