UniBoard Firmware Development Steps

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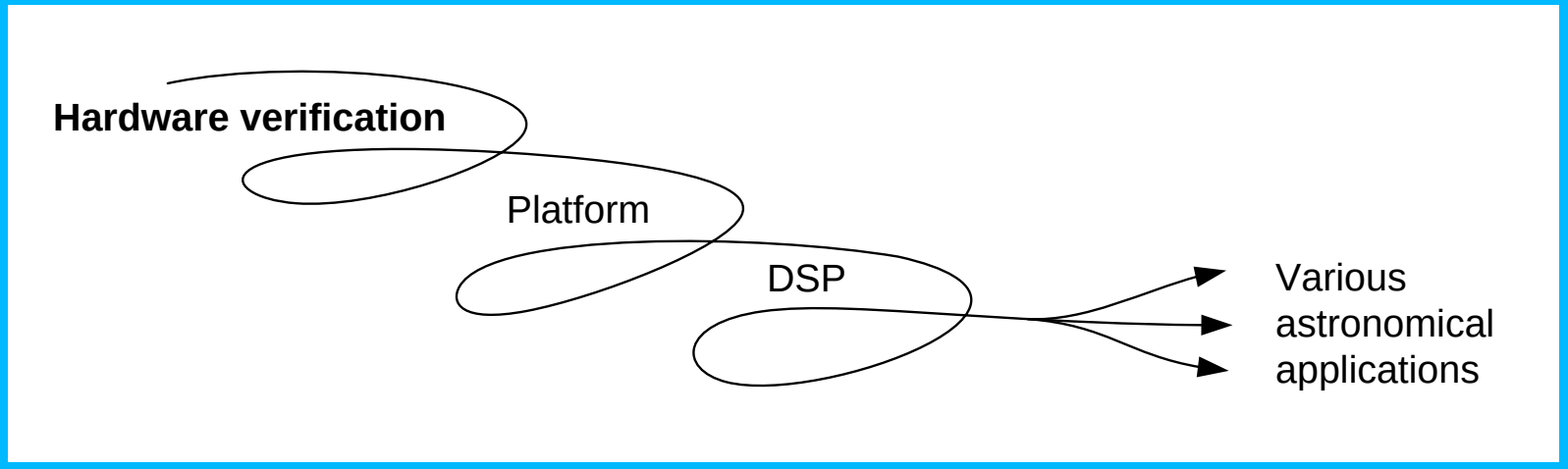
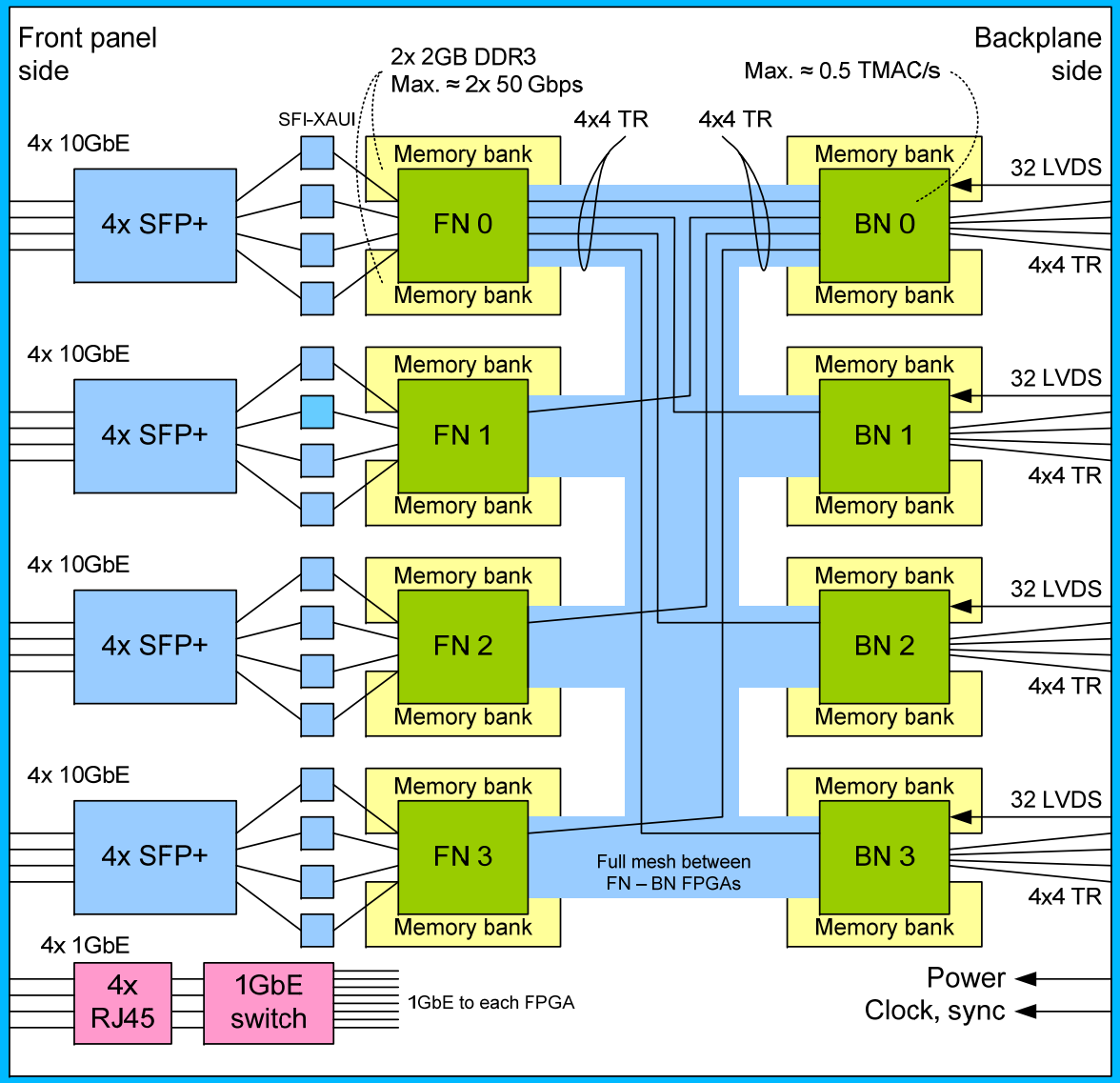


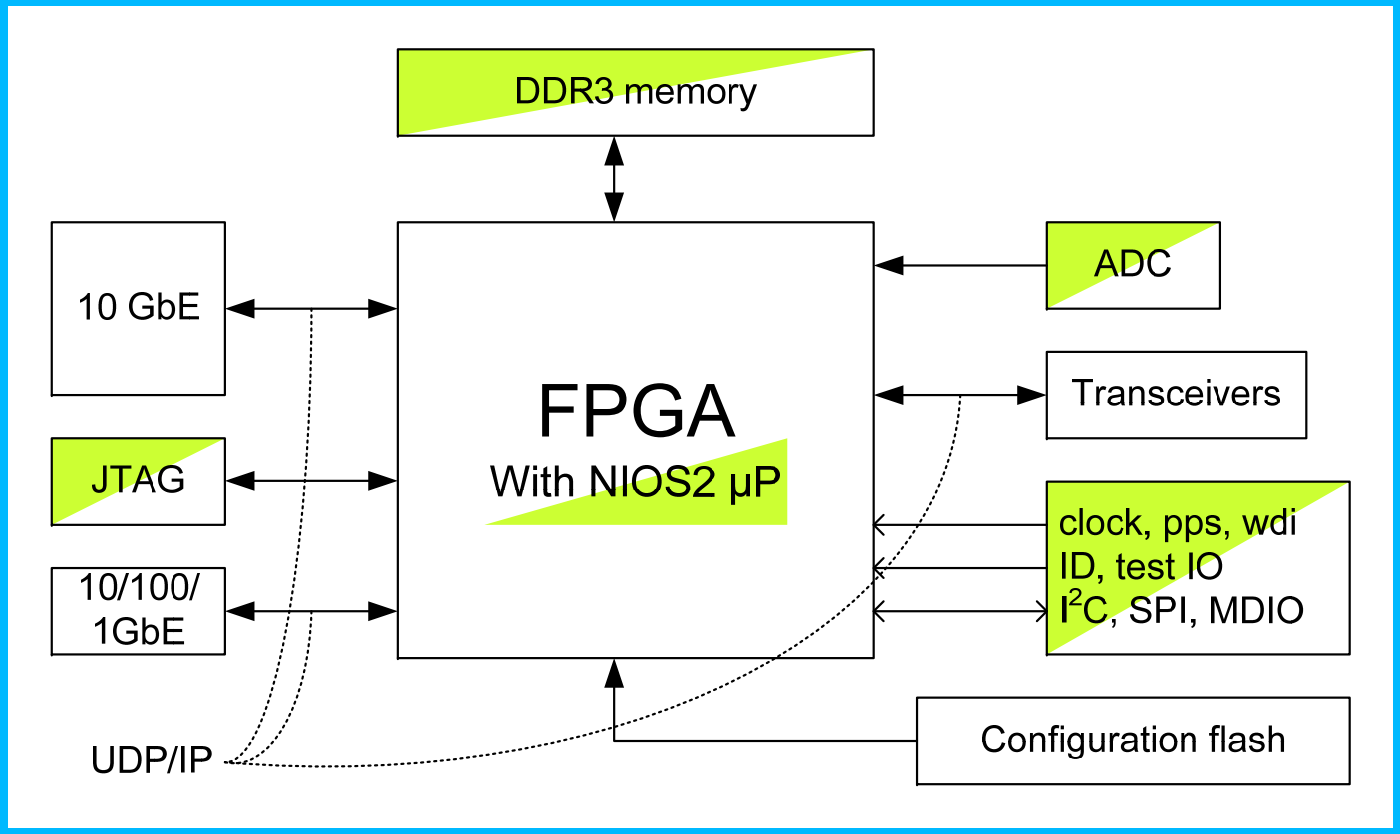
Hardware verification:

- Ongoing manual check with the Stratix IV documentation
- We have used Quartus II to check that the pins are used properly and we have estimate the power consumption
- Ongoing implementation of test firmware to verify the external interfaces of the FPGA in ModelSim and on target

UniBoard Block Diagram



Test Firmware Status Overview (dec 2009)



- For the green parts tests have been written in VHDL and/or C
- Aim is to have self tests for all interfaces when the target HW is available

Done

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- All FPGA pin assignments for both the back node and the front node have been verified with Quartus II synthesis and place & route using dummy firmware designs.
- The DDR3 self test and the I2C test for reading out the sensors can run in Modelsim as well as on target HW and report their results via the JTAG UART.

Ongoing

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- Plan is to (re)use UDP/IP packet based tests for 1GbE, 10GbE and the transceiver links.
- For UDP/IP we may run a stripped NicheStack on the NIOS2 soft core µP in combination with HDL streaming test packet generators and monitors.
- Improve the simulation test bench environment, aim is to be able to simulate all functionality, to ensure that it will run OK on target HW as well.

To do

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- ADC interface self test using pseudo random data generator
- Software for accessing the SPI flash (e.g. to store IP and MAC address)
- Software for accessing the MDIO control of the DDR3 and the 10GbE XAUI chips

- Control access via the 1GbE using UDP via the 1GbE switch

- More rigurous tests:
  - Raise speed of TR and DDR
  - Run test for hours, days, weeks
  - Combine IO tests with DSP to ‘fill’ the chip and run it hot