A 4 GHz digital receiver using the Uniboard platform

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ABSTRACT

The Uniboard is a general purpose board, developed as a part of the Radionet FP7 program, that hosts 8 Altera StratixIV FPGAs interconnected by high speed links. It can be used standalone or as a part of a more complex system.

The Digital receiver application uses a single Uniboard to implement a flexible packetization of a wideband signal in the frequency domain. It accepts a 4 GHz (8 GS/s) input bandwidth and provides up to 64 output bands. The bandwidth and position of each output band can be independently adjusted.

The input signal is first analyzed by a polyphase filterbank, that splits the input band into 32 sub-bands with a bandwidth of 190 MHz and a spacing of 128 MHz. The overlap among adjacent bands allows the positioning of the output bands without dead regions. This filterbank is followed by an array of digitally defined downconverters, each one composed of a mixer/LO and a variable decimation filter. The filter band can be adjusted in binary steps from 1 to 128 MHz. Using tap recirculation, the filter shape remains constant over this whole range, with about 60 dB of stopband rejection and 90% usable passband.

The output bands are packetized according to the VDIF VLBI standard, over eight 10G Ethernet links. Further processing can be done either on board, or in a cluster of conventional PCs.

In addition, high speed ADC are in-house developed (ASIC 65nm CMOS STmicroelectronics) to feed the Uniboard card with 8GS/s, 4GHz BW, 3bits samples.

Keywords: Digital signal processing, FPGA, radioastronomy, digital receiver

1. INTRODUCTION

Wideband receivers, with bandwidth of several GHz, are increasingly common in radioastronomy. The large bandwidth provides increased sensitivity, and simultaneous observation of widely spaced spectroscopic features. Direct digital processing of wideband signals is however difficult, and a digital system to decompose the wideband signal into channels of smaller, manageable bandwidth is useful for almost all radioastronomic applications. As a large portion of the band is usually affected by RFI, the possibility of processing only the clean portions of the incoming band is also very useful, provided that the system has sufficient rejection of out-of-band signals.

Here we describe a wideband digital receiver application, that decomposes a signal with a bandwidth of up to 4 GHz into many independently tunable channels, developed for the Uniboard platform. The Uniboard is a general purpose digital processing platform developed as a joint research project in the European Framework Program *Radionet*. It is described in detail in Ref. 1 in this conference, and its main characteristics are summarized in chapter 2. A number of applications have been developed for this platform, besides the one described here, including a VLBI correlator, a pulsar machine, a beam-former for LOFAR, and some RFI mitigation modules.

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2. THE UNIBOARD ARCHITECTURE

The Uniboard is a digital processing board based on Altera 28 μm StratixIV field programmable gate arrays (FPGA). Each board contains 8 large FPGAs, with each FPGA providing about 1100 18 bit multipliers that can operate up to a few hundred MHz, and 32 fast serial links that can be grouped into 8 fast lanes. The board total aggregate computing power is of the order of 2 teraops per board.

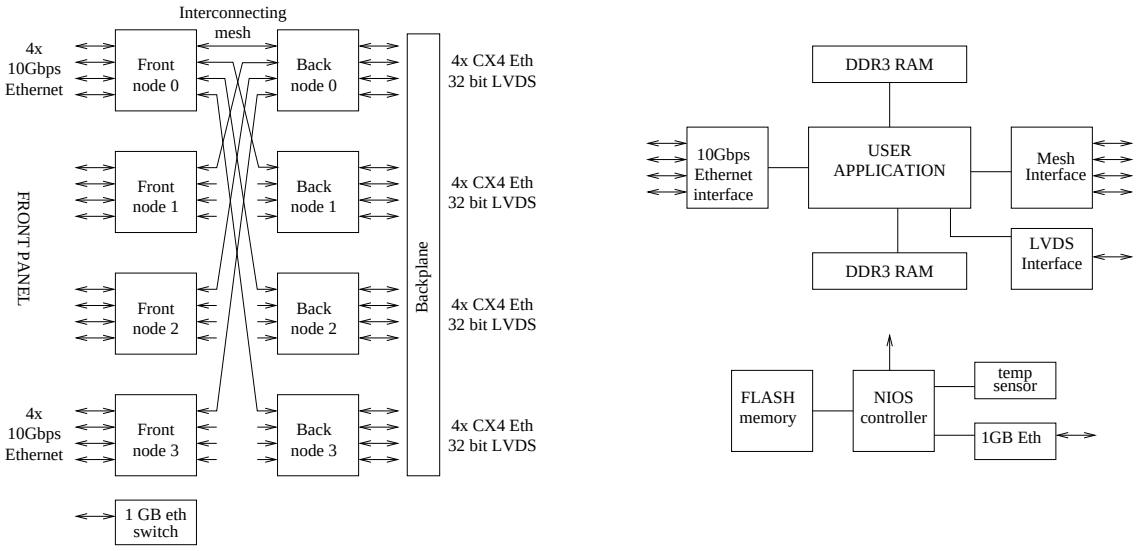

Figure 1. Structure of the Uniboard platform (left) and of each individual node (right). Board is composed of 8 FPGAs (nodes) interconnected by a fast serial net. Each node is composed of a set of common interfaces, a control processor and user defined logic

FPGAs are organized as 4 front nodes and 4 back nodes (fig. 1). Each front node is connected to each back node via a fast serial bidirectional data lane, with a datarate of about 20 Gbps. Each node has 4 10Gbps serial ports, the front nodes using an optical SFP+ transceiver, and the back nodes using a CX4 interface. Two banks of DDR3 memory are available for each node, in addition to the internal on-chip memory. The back nodes also have a parallel LVDS interface, that can be used to input samples from one or more fast ADCs, up to about 13 Gbyte/s.

The board can be used as a standalone unit, or as an element of a larger system. Several boards can be connected together using a backplane, with the CX4 ports providing point-to-point interconnection among boards, and the optical links interconnecting different racks or providing general input/output.

FPGA configuration personality can be downloaded using a JTAG interface, or stored in a FLASH memory under program control.

2.1 Common framework

A library of generic control modules, written in VHDL language, provides a common control framework for all Uniboard applications. These modules include a control processor in each FPGA, generic interfaces for the on-chip peripherals, and commonly used functions, like registers, safe crossing of clock boundaries, etc.

The 10G links can use either the IP/UDP protocol, or a custom point-to-point protocol, named *Uthernet*, optimized for simplicity and speed. The IP interface implements in hardware the ARP resolution protocol and ICPM ping capability. The IP address/port can be read directly from the UDP packet to be send, so apart from initialization it requires no interventions from the controller.

Each node contains a small controller, implemented with the Altera NIOS soft processor. The processor has several standard peripherals, including the personality FLASH memory, a voltage/temperature monitor and a

1000-base-T Ethernet interface. A commercial Ethernet switch interconnects the nodes, and allow them to be controlled using an external computer.

The NIOS processor runs a simple control/monitor program, that receives commands on the Ethernet interface, executes them and sends back a reply. Each programmable element in the system is implemented as a set of registers. Commands allow to write and read peripheral registers, either individually or in blocks, and any more complex, application specific functions are implemented in the external control computer.

The control protocol is extremely light. To avoid the overhead associated with the TCP protocol, the simpler UDP protocol has been used. Each command contains a unique tag, and requires a single response. The controlling computer can thus check for dropped commands or responses, and resend the command if this happens. The control program in each node checks for duplicate commands, and resends the response if necessary.

3. THE DIGITAL RECEIVER APPLICATION

A *Digital Receiver* is a system composed of a fast ADC and a set of filters, local oscillators, and mixers that extract the portion of the input signal of interest, decomposes it into several narrow-band channels, and transmits them, in digital form, to the data analysis equipment. In the most extreme case the ADC directly analyzes the sky frequency, without intermediate frequency conversion stages, while for higher observation frequencies the ADC digitizes the whole intermediate frequency band, with just a single conversion stage. The advantage of this approach is that all the phase uncertainties associated with analog filtering and frequency conversion are eliminated, and apart from the passband response of the ADC the system amplitude and phase responses are fully deterministic.

The task of decomposing a wideband signal into smaller bands using a digital system is usually performed with a *polyphase filterbank*.[2] This component divides the input signal into equispaced bands, using a FIR filter and a Fourier transform engine. This approach has the disadvantage of being extremely rigid: each band has the same width and its position is fixed. Moreover, due to the filter edge response, the edges of each band must be discarded, resulting in spectral holes between bands. It is possible to overcome this by overlapping the output bands, but at the expense of doubling their number, with a large penalty in data efficiency.

Using individually tunable filters, as for example in the correlator for the ALMA interferometer,[3] it is possible to place the individual output channels everywhere in the input band, with just a small overlap to discard the problematic edge regions. This allows for piecewise spectral analysis of wideband signals, reconstructing the seamless spectrum. When the whole input band needs not to (or cannot) be observed entirely, its interesting portions can be chosen without restrictions. For example it is possible to choose only the portions free from strong RFI, or containing interesting spectral features.

Wideband tunable filters are however quite expensive in terms of computing resources, requiring parallel processing of several consecutive samples. In this design we try to obtain the best from both approaches, using a polyphase filterbank in cascade with an array of tunable filters operating at a narrower input bandwidth.

3.1 General architecture

The basic structure of the application is shown in fig. 2. The input signal is first divided into equispaced overlapping bands by a polyphase filterbank. Then an array of digital baseband converters (BBC) select individual portions of each band. Each BBC has an independently programmable central frequency and bandwidth. The output of each BBC is then formatted and sent over one or more 10G IP ports.

The input signal from 1 to 4 ADCs is fed to the Uniboard using the backplane LVDS ports. A test signal can be internally substituted to the input signal, and used for diagnostic purposes.

Polyphase filter output bands have a nominal (Nyquist) bandwidth and sampling rate that corresponds to the FPGA operating clock frequency. To avoid spectral holes between these bands, filter spacing is half the sampling rate, resulting in a nominal overlap of 50%. The actual overlap of the passband is lower, about 41% the nominal band. This allows full freedom for tuning an output channel of up to 1/4 the polyphase output sampling rate anywhere in the input band, as shown in fig. 3. For an output bandwidth of 1/2 the polyphase sampling rate, the output channel position is moderately constrained by the limited overlap.

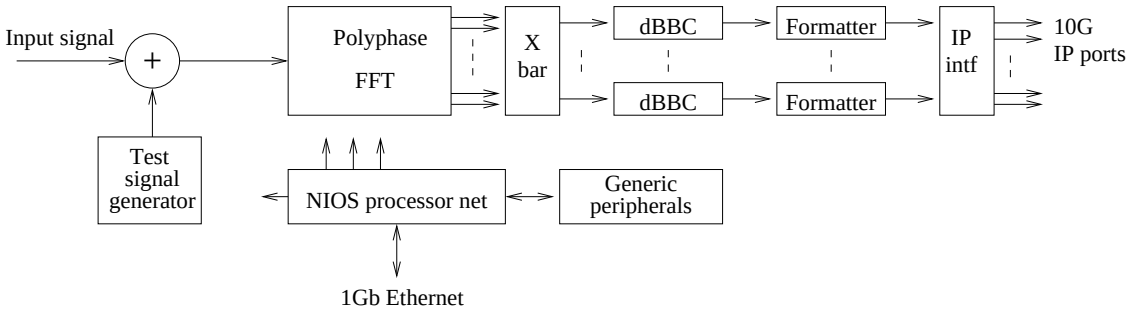

Figure 2. Structure of the digital receiver application. It is composed of a polyphase FFT, that initially divides the input band into 32 sub-bands, and an array of 64 DBBC, with individual VDIF formatters. The system is controlled by a network of NIOS embedded processors, communicating through a 1 Gb Ethernet

The large overlap allows to design the polyphase band with very large transition regions. For a 1/32 decimation (64 point FFT), the prototype filter has a total of 1024 taps, i.e. 16 taps per each Fourier transform input. A total of 256 multipliers per FPGA are required. Filter specifications are reported in chapter 5.

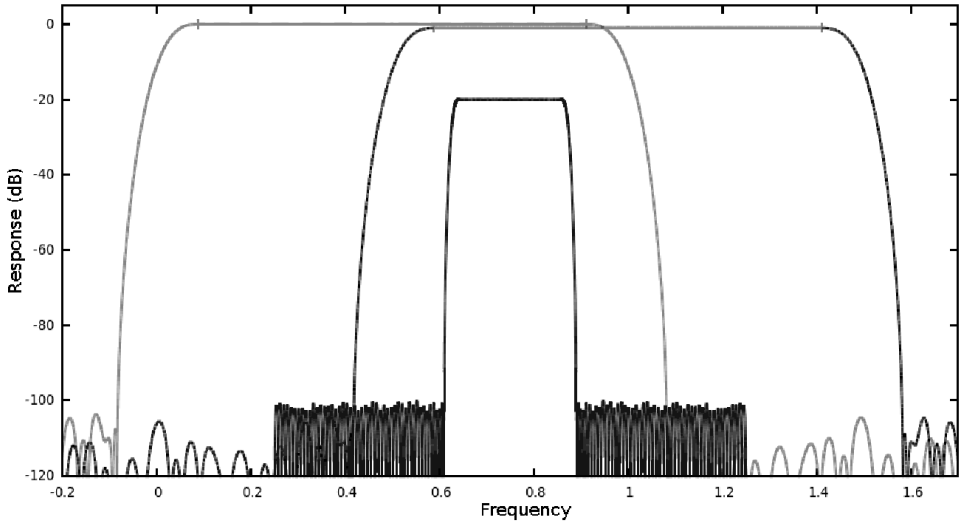

Figure 3. Bandshape of the polyphase channels (two adjacent channels shown) and of the output filter (decimation = 4, vertically shifted by -20 dB). Frequency unit is the polyphase output sample rate. The useful portion of each polyphase channel is marked by small vertical ticks

3.2 Specific applications

The digital receiver application discussed here has been tailored for the following astronomical applications:

- A VLBI data terminal, providing up to 64 channels arbitrarily positioned over a 4 GHz input bandwidth. Each channel may have a different bandwidth and output data coding (1 to 8 bit/sample), and output data is sent over the optical links to a storage device or an e-VLBI correlator as standard VDIF-over-UDP packets. This receiver will use a 6 bit ADC that is being developed by the University of Bordeaux; ADC project status is described in chapter 6.

  The VDIF packets can be also analyzed by a non-VLBI data acquisition system. A spectrometer based on generic graphics processing units (GPU), i.e. high-end computer video cards, is currently being developed for single dish spectroscopic applications.

- The same VLBI data terminal can be used with 4×1 GHz input channels, e.g. for double polarization dual band observations. 16 output channels, identical to those of the previous case, are available for each input signal. Each of the 4 receivers fit in a single back node, leaving the front nodes for other purposes (e.g. RFI mitigation, and/or wideband spectroscopy).

- A pulsar formatter, splitting a total 3.1 GHz dual polarization bandwidth into 80 dual polarization channels of 20 MHz each (160 total). Only a subset of the input band, tailored to avoid strong RFI, is covered by the receiver. Each output channel has a similar structure with respect to the previous case but, due to their much larger number, the available number of taps and the filter performances are reduced.

  Channels are sent as custom formatted UDP packets to two data analysis computers using the optical links. These computers use a bank of eight GPUs each to perform pulsar coherent de-dispersion and accurate timing over the analyzed band.

4. IMPLEMENTATION

The system is physically distributed over the 8 FPGAs composing the board, except for the 1 GHz version that fits in a single back node. The 4 back node FPGAs implement the test signal generator, the filter section of the polyphase filterbank and the first 4 stages of the FFT, while the 4 front node FPGAs implement the last stages of the FFT, the DBBCs, and the formatter/IP layers.

The design will use the general framework developed as part of the Uniboard project. Standard components will be used for FPGA-to-FPGA intercommunications, IP formatting, and for the standard control structure. Generic peripherals for the NIOS processor use Altera library modules.

4.1 Polyphase filterbank

A polyphase filterbank is a structure in which a Fourier transform is preceded by a set of finite impulse response (FIR) filters.[2] The structure effectively convolves the input of the Fourier transform with an appropriate tapering function, allowing to control the shape and insulation of the filterbank output channels. It can be considered as a standard low-pass filter, which response is transposed in frequency around a set of uniformly spaced frequencies by the Fourier transform operation.

The polyphase filter is implemented in a distributed way across the back node FPGAs. The 4 GHz design uses all 4 back nodes, and the pulsar design uses 2 back nodes per polarization. The last 1 or 2 stages of the polyphase FFT, combining together the outputs of different back node, are implemented in the front nodes. The input signal is multiplexed in time, with N consecutive samples presented in parallel as N data streams to the filterbank. Samples are presented in bit-reversed order: this comes naturally if successive time multiplexing is done in cascade. In particular, successive samples from the ADC are sent to different FPGAs.

The complete structure of one back node FPGA is shown in fig. 4 (single 4 GHz receiver case, N=32). Sample numbers refer to the first FPGA, the other FPGAs process samples offsetted by 1, 2 and 3 ADC sampling periods. A total power meter measures the power level in the input signal, and for each filterbank output.

Each data stream is processed in two short FIR filters (fig. 5), that produce at each clock cycle two filtered samples, with indexes i and i+32. As the data rate is doubled with respect to a conventional polyphase filterbank, on odd clock cycles a phase slope is introduced in the data by the filter. To remove this, on odd cycles samples i and $i + 32$, that are produced by the same filter branch, are exchanged.

Filter outputs are analyzed by a division-in-time fast Fourier transform engine of size $2N$. As the input signals are real, only N FFT outputs are independent and need to be carried on, with each output containing informations both for channel n and $N - n$. The real outputs for channels 0 and N are combined together in a single complex signal.

Due to limited bandwidth between the front and back nodes, FFT outputs are re-quantized to fewer bit quantities, 9 to 12 bit signed, depending on the number of FFT outputs and sample frequency. Individual outputs are re-quantized at an optimal quantization step, depending on the measured power in that output. This truncation between FFT stages result in a non perfect cancellation of the signal outside the channel passband.

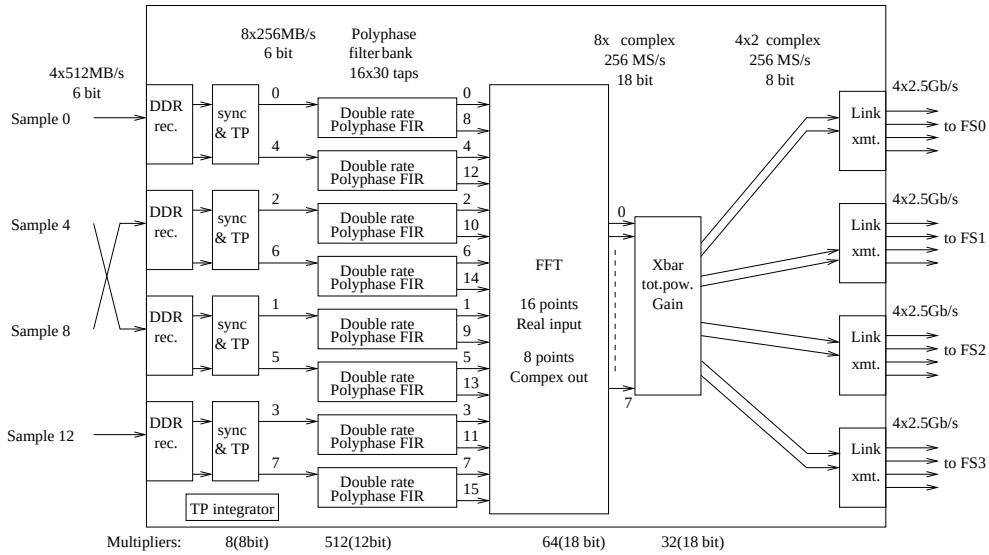

Figure 4. Structure of the input FPGA

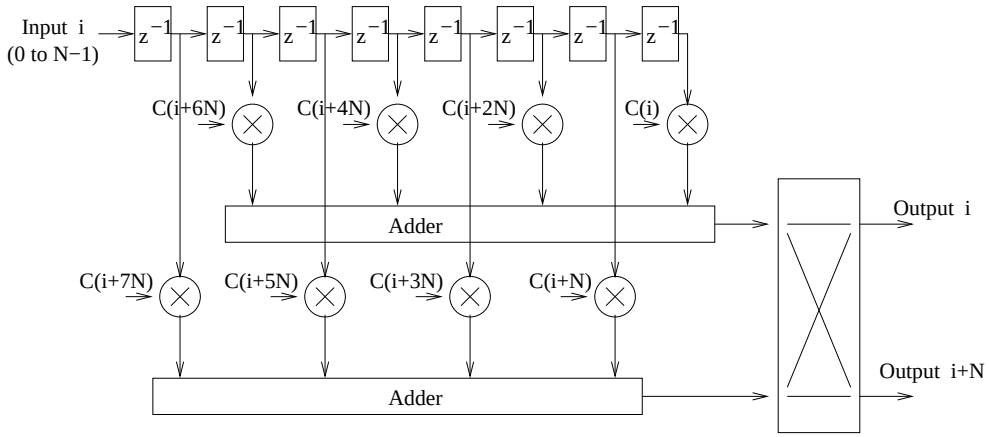

Figure 5. Double rate polyphase filter branch. On odd cycles the two outputs are exchanged, to remove phase slope. Only 4 taps per branch are shown, actual filter has 16 taps per branch

As the signal is basically Gaussian noise, however, cancellation occurs on a statistical basis, and rejection is much higher than that expected for a deterministic signal. Simulations with realistic signals have been used to assess actual stopband rejection. Values around 75 dB are achieved for 9 bit quantization in the interconnecting mesh, and more than 95 dB for 12 bit quantization.

The final stage of the $2N$ size FFT is implemented in the front nodes. The algorithm exploits the complex conjugate relation between channels n and $N - n$, computing just the necessary operations. The special case of channel 0 is treated separately (fig. 6).

Each front node computes only a subset (typically 1/4) of the total polyphase filterbank outputs. This limits the flexibility of the system, especially when the channels represent portions of the input band of different astronomical interest. It is however possible to choose, with some limitations, the distribution of bands among front nodes, and even to avoid to process a particular set of bands. This has been extensively used in the pulsar receiver application, in which some bands are filtered in the front end because of heavy RFI contamination and need not to be analyzed.

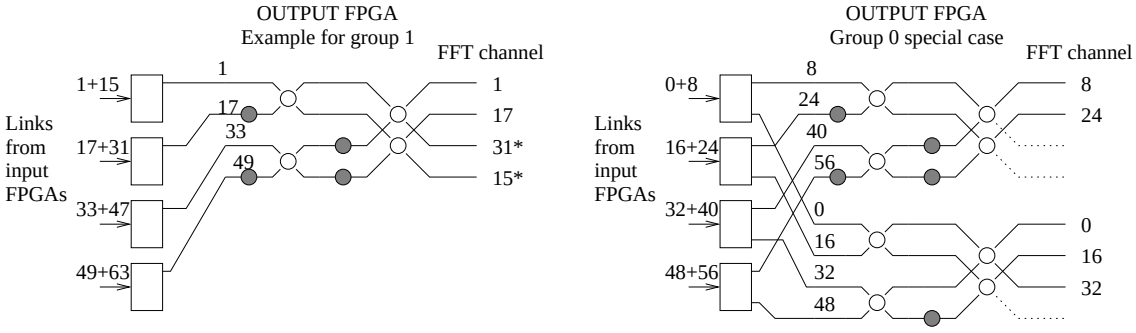

Figure 6. Output stage for 32 channels FFT. a) generic block, b) special case for channel group 0.

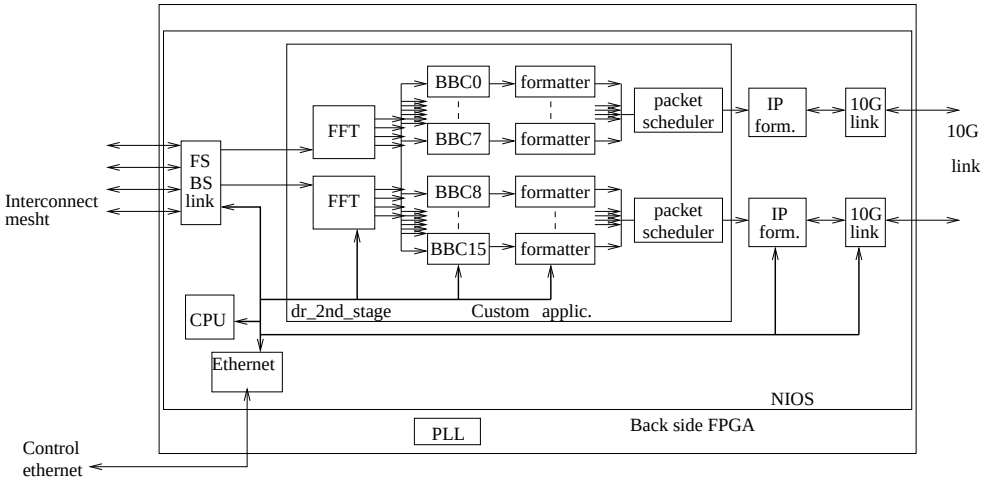

Figure 7. Structure of the output FPGA (4 GHz, 64 channels version of the digital receiver)

4.2 Digital baseband converter

The polyphase filterbank outputs present in a front node are analyzed by an array of *baseband converters* (BBC). Each BBC is composed of a complex oscillator/mixer, that sets the center frequency of the selected band, a low pass filter and a complex-to-real conversion stage.

The filter band and decimation factor define the channel output band, that ranges from 1/2 to 1/256 of the clock frequency. For a real output, the sample frequency is twice the nominal bandwidth (Nyquist sampling). If the complex-to-real stage is omitted, the output format is complex, and the sample clock rate is further divided by 2.

The filter is implemented as a symmetric finite impulse response, with tap recirculation. The total number of multipliers is fixed and operates always at the maximum speed. The filter length is thus proportional to the decimation factor, and the filter shape remains roughly constant (same fraction of usable output bandwidth) and does not degrade with the decimation factor.

A last total power meter and rescaling stage is used to adjust the signal level, and the output is re-quantized to 8 bits. The output level spacing is chosen with a threshold across zero, and equally spaced levels. This means that code i represents an interval of possible values centered at $i + 1/2$, and allows to re-quantize the signal by just discarding the least significant bits of the sample code.

4.3 Formatter and IP interface

The signal from the individual BBCs is then packed in a format appropriate to the specific application. For generic radioastronomic data, either single dish or interferometric, the VDIF format[4] has been used. In this format the

samples from the BBC are quantized to 1, 2, 4 or 8 bits per sample, and an header specifies informations about the absolute time, the quantization, an identifier for the station and the data thread, the frame length, and the bandwidth.

For the pulsar receiver, data are packed in frames of 8 Kbytes, with 1 to 16 complex signals in double polarization, 8 bit per (real) sample, i.e. 4 to 64 bytes per sample period. Time is implicitly specified by consecutively numbering each frame, and recording the starting time of the first frame.

Data is always encapsulated as UDP packets, with programmable destination UDP port and IP address. Maximum packet length is 8 kbytes, i.e. near the limit for a standard Jumbo IP frame. A packet scheduler and IP interface selects the first ready packet from a set of formatters and send it over a specific 10G optical link. Up to 12 of the 16 board optical links can be used in this way, allowing for a maximum raw data bandwidth of 15 Gbyte/s.

5. FILTER SPECIFICATIONS AND DESIGN

Filter specifications for the polyphase and output filters are summarized in table 5. The output bandwidth is expressed in terms of the output sampling rate, i.e. is 100% for an ideal rectangular filter. Passband ripple is expressed as decibel peak-peak.

Filter	Decimation	Band	Passband ripple	Stopband atten.	N. of taps
Polyphase	32(8)	82.5%	0.007 dB	> 102 dB	1024(256)
VLBI output	$N = 2 - 256$	88%	0.036 dB	82 dB	$32N$
Pulsar output	8	82%	0.036 dB	83 dB	176

Table 1. Characteristics of the input polyphase filter (4 GHz and 1 GHz) and of the output band shaping filters

The polyphase filter shape has been determined by a desired stopband attenuation of 100 dB, and by the requirement of an overlap wide enough to accommodate at least a decimated by 4 BBC channel. A large overlap is useful also for smaller BBC channels, as the extra freedom allows to better share the output channels among different front node FPGAs.

The BBC filter shape is determined by the desired stopband attenuation, that has been fixed to 82 dB, and the number of available multipliers in the FPGA. For the 4 GHz receiver, an usable bandwidth of 88% of the nominal (Nyquist) band has been achieved, corresponding, for example, to 56 MHz for a 64 MHz nominal band. The pulsar receiver has a much larger number of individual output bands, resulting in a usable band of 82% of the Nyquist frequency (20 MHz per channel).

Filters have been designed using the Remez algorithm. This algorithm presents numerical problems for very large number of taps (up to 8192 for the VLBI output filter). Therefore the largest filters have been computed by interpolating the response in the time domain of smaller filters, and adjusting the extreme tap coefficients.[5] This results in a very accurate scaling of the filter response to higher decimation factors, as shown in fig. 8.

6. 5 AND 8 GHZ ADC MODULES

A digitizer module based on commercial ADC from E2V has been designed and fabricated at the LAB of the Bordeaux University, where it is currently under test. This module implements 2 ADC, generating 5GS/s of 10bits and a Stratix IV FPGA (same model used in the Uniboard). This FPGA is used to capture the data transmitted from the ADC as 4 channels (4×10 lines per ADC) at 1.25GHz and to perform basic signal analysis. The signal can be further transmitted to the Uniboard using 16 transceivers operating up to 6.5Gb/s for complex digital signal processing. Although the interleaved band is 5 GHz, the analog band is limited to 3 GHz, and the unit will be mainly used for engineering tests.

Full custom ASIC are also being designed. A 8GS/s 3 bits digitizer will be fabricated during summer. It is based on 65nm technology from ST-microelectronics. This digitizer implements in a single chip a Track and Hold (8GHz bandwidth) and ADC using a FLASH architecture. To optimize the transmission from this ADC

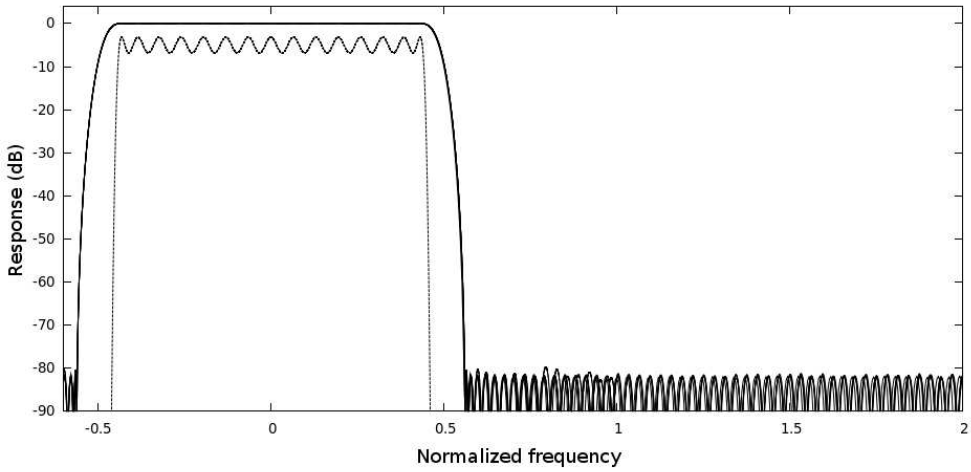

Figure 8. Passband of the BBC filters, for decimation between 2 and 256, normalized to the output sampling rate. Apart from details of the stopband, the filter shape scales exactly as the output sampling rate. Dashed curve is the passband magnified by 1000 times to show the passband ripple

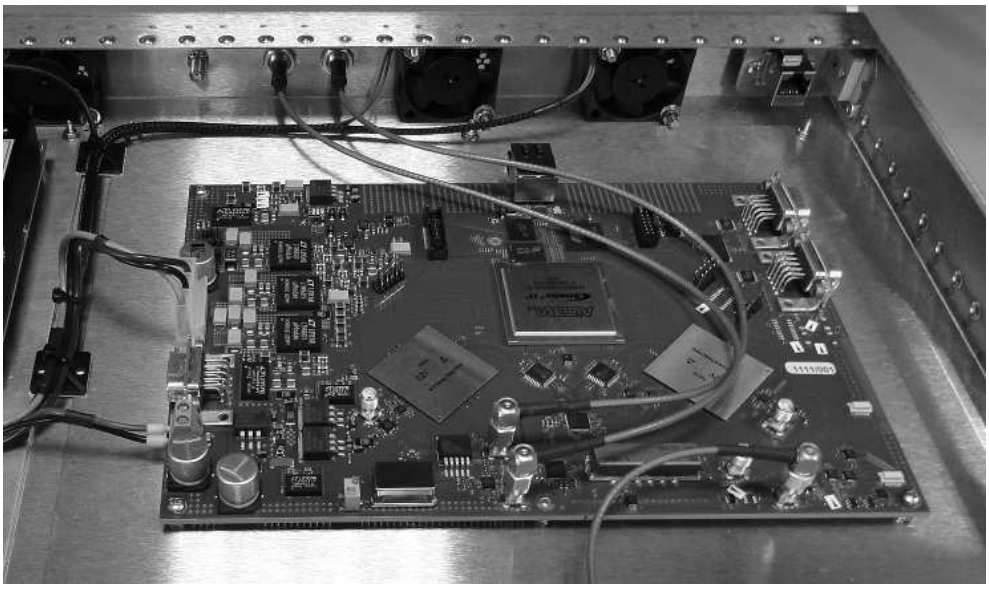

Figure 9. 2×5 GS/s ADC module being developed by the LAB-Bordeaux

to the Uniboard, pseudo random sequence generators operating up to 8Gb/s have been designed with the same technology. They can be used to synchronize the transmission between ASIC and FPGA and to scramble the data to increase the commutation rate as required by the high speed serial transmission.

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