Investigating Model Based Design Vs VHDL based Modular Design (status update)

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Evaluation

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- Evaluation attributes
  - Development Time
  - Testing Time and Quality
  - Reconfigurability
  - Optimization Flexibility
  - Reusablilty
  - Chip occupancy
- Target Users
  - Physicist
  - Engineer
  - Student
- Demo Application
  - Applicable DSP Block for quantitative evaluation : FFT
  - Application : APERTIF, however block is designed for reuse.

Chronology : Past

- W39:Sep2009 : Mathworks SIMULINK HDL Coder and all additional packages installed.
- W40:Sep2009 : CASPER Workshop
- W42:Oct2009 : OTHER
- W43:Oct2009 : OTHER
- W44:Oct2009 : Literature review FFT + elementary VHDL modules
- W45:Nov2009 : VHDL design for pipeline FFT (R2SDF)
- W46:Nov2009 : OTHER
- W47:Nov2009 : OTHER
- W48:Nov2009 : OTHER
- W49:Dec: 2009 : R2SDF design completed with synchronization
- W50:Dec: 2009 : Testing R2SDF FFT

Chronology : Future

- W51:Dec: 2009 : Other
- W52:Dec: 2009 : Other
- W53:Dec: 2009 : Testing R2SDF FFT
- W01:Jan: 2009 : Vacation
- W02:Jan: 2009 : Vacation
- W03:Jan: 2009 : Vacation
- W04:Jan: 2009 : Other
- W05:Feb: 2010 : Other
- W06:Feb: 2010 : Other
- W07:Feb: 2010 : R2SDF Test + Module completion
- W07:Feb: 2010 : R2SDF Test + Module completion

Conclusion and Discussion

- Current Status

  FFT : R2SDF VHDL coding is complete
  Library : FIFO, Cmplx Arthemetic, Mux, De-Mux.
  : tested, ready and synthesisable
  MBD : tool flow is understood and through with preliminary learning phase.

- Next Steps

  FFT : R2SDF Testing using LOFAR VHDL testbench.
  Library : consolidate components for re-use
  MBD : design and test R2SDF pipeline FFT using Simulink Blocks.

- Discussion...