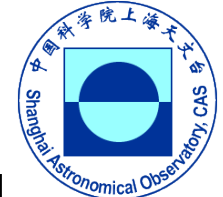


# Chinese VLBI Data Acquisition System

Rongbing,Zhao



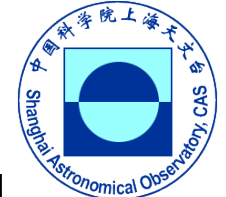
# CDAS OVERVIEW



CDAS is FPGA based VLBI data acquisition system . There are four IF inputs in CDAS. Each IF input could be 50 ~ 1024MHz frequency range. CDAS selects 50 ~ 512MHz or 512 ~ 1024MHz signal as exactly used signal to do processing. For 512MHz bandwidth signal, CDAS could extract up to 32 sub-channel data streams with different bandwidth, different central frequency and different output bit length. With these feasibilities, such as broad bandwidth input, flexible band central frequency choosing and convenient band width selection, multi-bits data streams output, CDAS provides major improvement feasibility for CVN observations. The main parameters of CDAS are described in Table



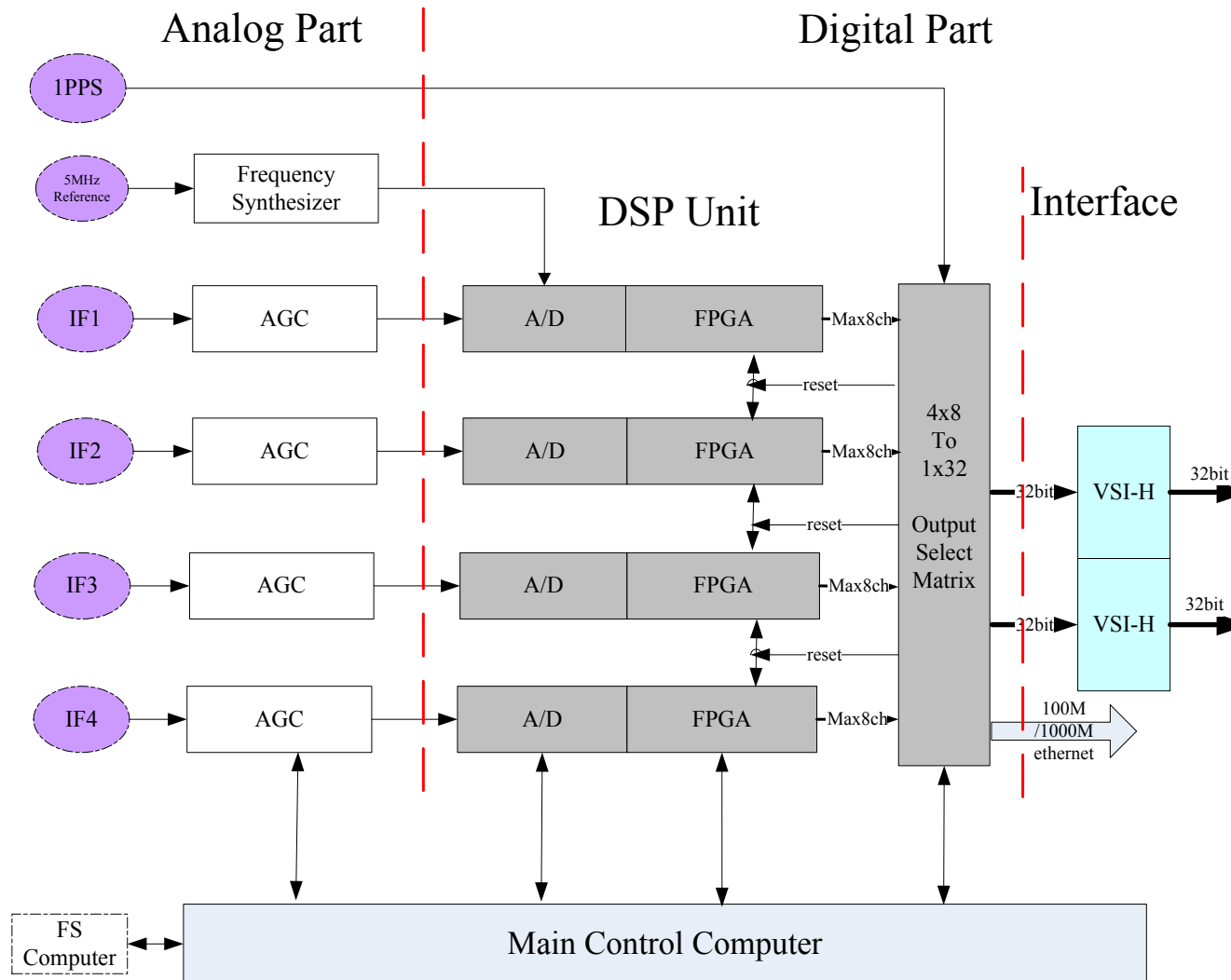
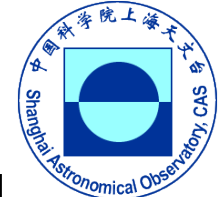
# Parameters of CDAS



Parameters	Value
IF input frequency	50 ~ 1024MHz 512MHz/512~1024MHz/ 10~1024MHz
IF channels	Up to 4
IF input power level	-44~ -4 dBm
IF sample rate	1024Msps
Reference frequency	5MHz
Reference frequency power level	7 ~ 13 dBm
Base band channels	Up to 32
Base band frequency resolution	10 KHz
Base band bandwidth	0.5,1,2, 4, 8, 16, 32MHz
Base band sample bit	1,2,4,8 bits



# System Structure and Configuration





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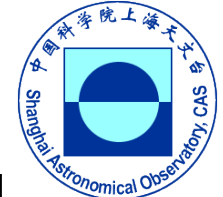
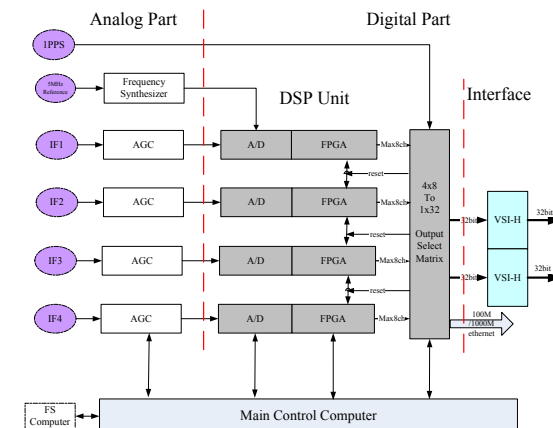


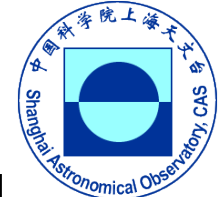
Figure shows the overview of CDAS System. Via AGC module, the amplitude of IF input signal will be stepped control to suit the ADC requirement. Under the control of the command of CDAS, low or high IF signal could be selected to process. The maximum dynamical range of amplitude is 60dB with minimum delay change during the amplitude adjusting. The main control computer which belongs to the digital part is responsible for the whole system communicating with Field System (FS) computer, command the system and diagnostic the status of CDAS during the observation time.

Like most other digital VLBI data acquisition system, approach to 'ADC + FPGA' is adopted for CDAS which composed of analogy part and digital part. The analogy part is responsible for anti-aliasing and AGC (Automatic Gain Control) which has about more than 40dB dynamic range of input power level from -44dBm to -4dBm in order to fitting for tracking spacecraft and keep the optimal quantization level for the following ADC.

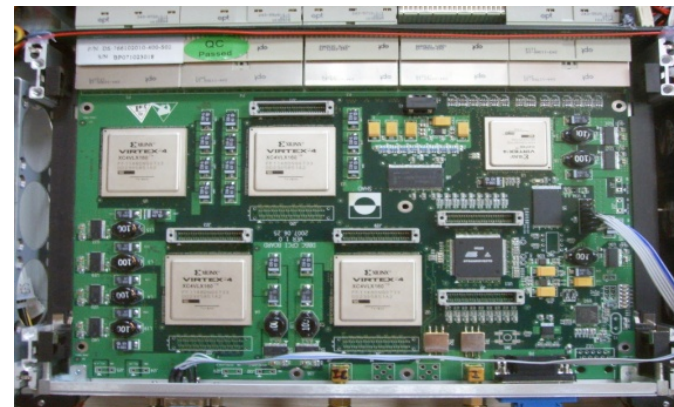
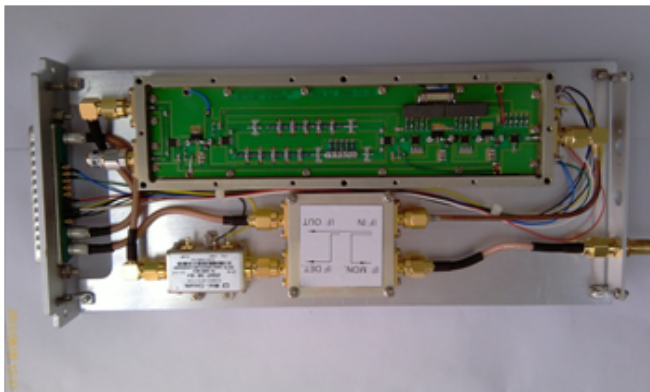




# System Structure and Configuration

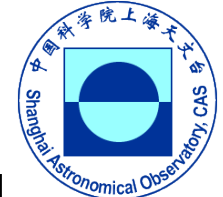


The CDAS analogy part consists of four AGC modules, one system clock generator and one control module. Each module is integrated in an individual box, which has perfect EMC characteristics. All of such modules are installed in a 19 inches chassis with power supply. Figure 2 and Figure 3 show the pictures of analogy part and digital part of CDAS separately. The digital part is responsible for data acquisition and process. The main hardware of digital part is two PCB boards which are developed by SHAO. One of these two PCB boards is an interface board. This board has a VSI-H interface which can be connected with MK5B recorder. Another of these two PCB boards is so named DSP unit which included two channel 1Gbps Analog to Digital convertor and four large scale FPGAs in daisy chain. The digitizing of each IF signal and processing the signal is completed in real time in this DSP board. The signal processing are including Direct Digital Frequency Synthesis (DDS), digital down convert, filters and power level calculating etc. Each DSP board could process one IF input signal.



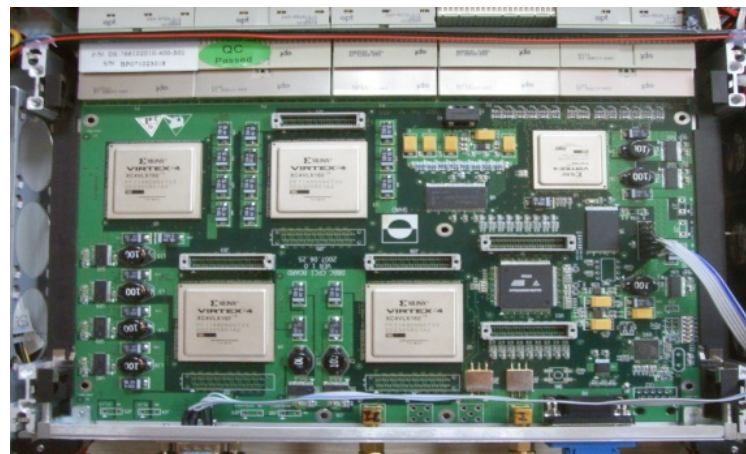


# System Structure and Configuration



Each FPGA on the DSP board could produce one BBC including both USB and LSB. The output data length of BBC is 8 bits. There are four DSP boards in CDAS which are used to processing four IF input signals. The output results of these four DSP boards would be sent to an output select unit which includes a 128 to 32 cross switch and re-quantification module. According the command of CDAS, the quantification module will determine the output bits number of sub-channels. The output bits number could be from 1 to 8 bits. On the basis of the command of CDAS, via cross switch, the system could select required sub-channels in required order to compatible to different VLBI data format. Such sub-channel data streams could be sent to Mark 5B system via interface board.

Figure 5 shows the photo of DSP board. This is a 6U standard Europe PCB board with c-PCI interface. There are one ADC (AT84AD001B, dual 8-bit analog –to-digital converter, Atmel) and five FPGAs on the board.





# Analog AGC Module

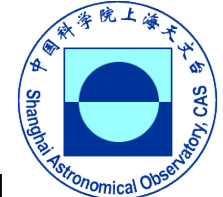
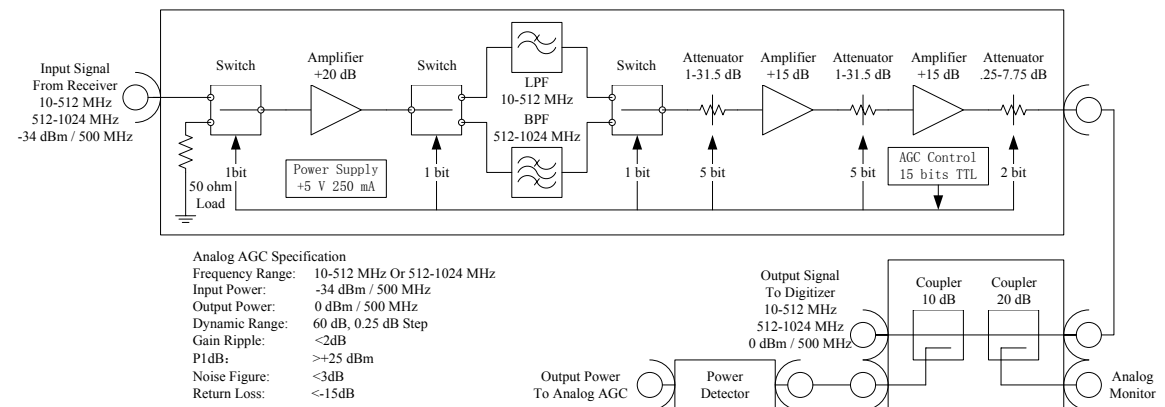
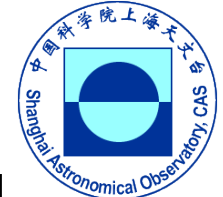


Figure shows the diagram of AGC module. The CDAS could be used to observe radio source and spacecraft. The signal power of spacecraft has large dynamic range during they go away from earth to deep space. Automatic gain control (AGC) is necessary for station receiver and backend system. Normally, it should be an adaptive [system](#). The average output signal level could be [fed back](#) to adjust the [gain](#) to an appropriate level for a range of input signal levels. The system delay will be changed following the value of fed back. Concerning to reduce the variance of system delay and phase during target signal changing, the 'amplify + [attenuator](#)' combinations are used for system gain control. The advantage of this combination could be maxim reduce the change of system delay. We used three amplifies, one has 20 dB gain and two has 15 dB gain each, and three adjustable attenuators with 60dB total decrement. There are a network which is configured with two microwave switchers, one low pass filter and one band pass filter. The function of this network is selecting low or high IF signal to process by command. The same delay values are also required for low and high pass. Figure 6 shows the curves of Gain / Frequency characteristics of four AGC modules in lower IF mode. Under the control of the command of CDAS, it could select low or high IF signal to process. Via AGC module, the amplitude of IF input signal will be stepped control to suit the ADC requirement. The maxim dynamical range of amplitude could be 60dB with minimum delay change during the amplitude adjusting.

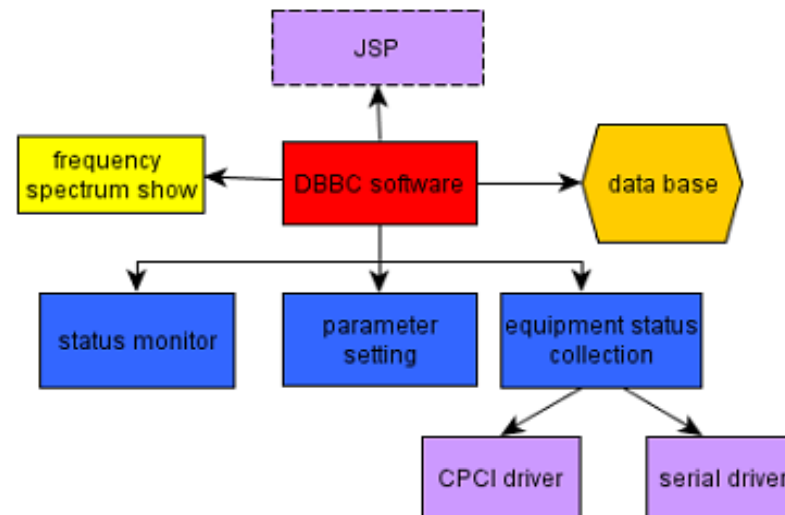


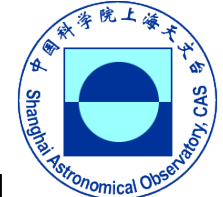




# CDAS Control Software

The software can control digital converter, AGC and output of CDAS and monitor their status based on the user command. Furthermore, the software also receives the command from FS system and transfer the status of CDAS to the FS.





# CDAS Control Software

The main window  
monitor its  
There are  
status show  
plot. The r

The screenshot displays the CDAS Control Software interface with several windows open:

- digital agc**: A table showing AGC parameters for various channels (bbc1 to bbc13).
- message show**: A log window displaying system messages and timestamps.
- FPGA Setting**: A configuration window for FPGA parameters, including ULSB, Band width, BitWidth, Frequency, and StartPhase.
- DBBC Control**: A window for controlling the DBBC (Digital Baseband Control) system.

The **digital agc** window contains the following data:

bbc	agc	mode	upower	dispower	upmax	downmax	uphit	downhit	upthreshold
bbc1	0	0	178961	174577	2223	2074	0	0	389
bbc2	0	0	179054	174579	2158	2114	0	0	389
bbc3	0	0	178925	178809	2223	2074	0	0	389
bbc4	0	0	179041	174570	2234	2150	0	0	389
bbc5	0	0	149142	147880	1977	2007	0	0	355
bbc6	0	0	149225	147961	1942	1894	0	0	355
bbc7	0	0	149139	147844	1862	1948	0	0	355
bbc8	0	0	149096	147895	1961	2021	0	0	355
bbc9	0	0	216558	213130	2411	2459	0	0	355
bbc10	0	0	216664	213247	2377	2265	0	0	355
bbc11	0	0	216399	213115	2395	2298	0	0	355
bbc12	0	0	216518	213241	2459	2310	0	0	355
bbc13	0	0	181504	177265	2129	2103	0	0	355

The **message show** window displays the following log messages:

```
10:24:30-10:24:30:is loading !
10:24:57-10:24:57:Done is high No CRC error.system is working normally!
10:24:58:aid reset success
10:24:58:reset synboard
10:25:04:32m reset success
10:25:04:reset synboard
10:25:06:filter reset success
10:25:06:reset synboard
10:25:57-10:25:57:is loading !
```

The **FPGA Setting** window shows the following parameters:

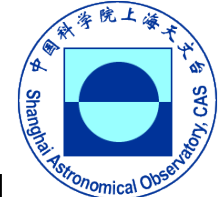
ULSB	Band width	BitWidth	Frequency	StartPhase	Set
USB	2m	1	606.990000	0.00	Set1
USB	2m	1	606.990000	0.00	Set2
USB	2m	1	606.990000	0.00	Set3
USB	2m	1	606.990000	0.00	Set4
USB	2m	1	606.990000	0.00	Set5
USB	2m	1	606.990000	0.00	Set6
USB	2m	1	606.990000	0.00	Set7
USB	2m	1	606.990000	0.00	Set8
USB	2m	1	606.990000	0.00	Set9
USB	2m	1	606.990000	0.00	Set10
USB	2m	1	606.990000	0.00	Set11
USB	2m	1	606.990000	0.00	Set12
USB	2m	1	606.990000	0.00	Set13
USB	2m	1	606.990000	0.00	Set14
USB	2m	1	606.990000	0.00	Set15
USB	2m	1	606.990000	0.00	Set16

The **DBBC Control** window shows the following parameters:

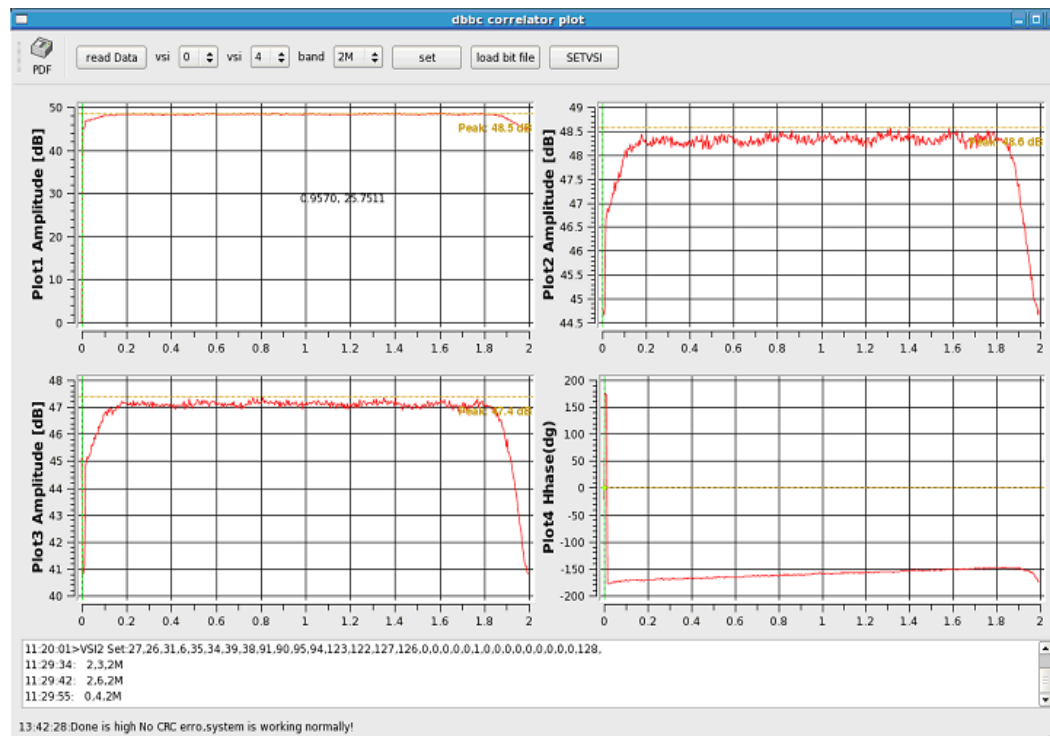
IFB	lock	atten	H/Low	agc
IFA	lock	6.00	HRASS	ma
IFB	lock	6.00	HRASS	ma
IFC	lock	27.00	HRASS	ma
IFD	lock	27.00	HRASS	ma



# Software Spectrum Monitor

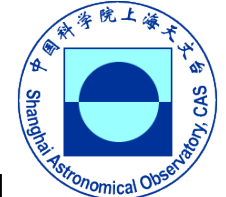


You can select two channels data to plot the autocorrelations and cross-correlation including amplitude and phase (see Figure). In the plot window, the figures show the autocorrelation of channel 1 and 2 and w the amplitude and phase of cross correlation.





# About the drudge



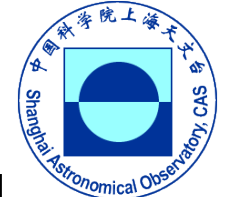
We modified the drudge software ,add the cdas rack to support the CDAS mode setting.

- 1.Add the the 64mhz external frequency support
- 2.Support the receiver high Lo and Low Lo mode
- 3.Add new mode vlba\_c

```
firstlo= 9100,9100,9100,9100,9100,9100,9100,9100,9100,9100,9100,9100,9100,9100,9100
ifchan  = A, C, A, C, A, C, A, C, A, C, A, C, A, C, A, C
bbc     = 1, 5, 1, 5, 2, 6, 2, 6, 3, 7, 3, 7, 4, 8, 4, 8
format = MARK5B   station = SHANGHAI /
```



# Cross Switch

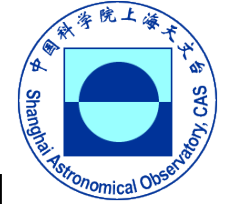


BS	vlba	vlba_c	
	FS/DBBC	FS	DBBC
0	1US	1US	1US
1	1UM	1UM	1UM
2	2US	2US	5US
3	2UM	2UM	5UM
4	3US	3US	2US
5	3UM	3UM	2UM
6	4US	4US	6US
7	4UM	4UM	6UM
8	5US	5US	3US
9	5UM	5UM	3UM
10	6US	6US	7US
11	6UM	6UM	7UM
12	7US	7US	4US
13	7UM	7UM	4UM
14	8US	8US	8US
15	8UM	8UM	8UM

16	1LS	1LS	1LS
17	1LM	1LM	1LM
18	2LS	2LS	5LS
19	2LM	2LM	5LM
20	3LS	3LS	2LS
21	3LM	3LM	2LM
22	4LS	4LS	6LS
23	4LM	4LM	6LM
24	5LS	5LS	3LS
25	5LM	5LM	3UM
26	6LS	6LS	7US
27	6LM	6LM	7UM
28	7LS	7LS	4US
29	7LM	7LM	4UM
30	8LS	8LS	8US
31	8LM	8LM	8UM



# CDAS Installation



Since year 2009, CDAS has been equipped in Shanghai, Beijing, Kunming and Urumchi VLBI station includes of FS Computer, Mark5B, and a LCD monitor. After integration in station, the firmware and software of CDAS have been updated for several times to improve the performance and correct the bugs.

