DBBC2 and DBBC3 report

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DBBC2:

New releases of DDC v106/E, PFB v16, FILA10G v4.

DDC v106/E

This new version includes the following modifications with respect to the previous one:

1) Supports Digilent programmer

2) Supports ADB3L*1

3) New 'cont_cal' command, now support different on/off frequencies in the range 8Hz - 300KHz

4) New mode 'geo2' with 16 USB on VSI1, 16 LSB on VSI2

PFB v16_1

The new version includes the following modifications with respect to the previous versions (v15 and v16)

1) Supports ADB3L*1

2) Support for Digilent FPGA programmer

3) 'FULL AUTO' mode in 'DBBCFORM' for full band mode with magnitude automatically controlled (requires CoMo TP optimization)

4) 'CONT_CAL' command for continuous noise cal settings

5) 'POWER_CONT' command for continuous TP measurements, now support different on/off frequencies in the range 8Hz - 300KHz

6) 'CALIB_VSI' command for optimize the intra-stack data output propagation

7) 'PCAL_DETECT' for phase cal tone measurements

8) 'STAT_COUNT' for statistics of the stats measurements

9) Post frequency conversion detector selection for the Conditioning Modules AGC control

FILA10G v4

1) Improves VSI output

2) Correction of bugs

DBBC3:

Hardware versions complete for systems:

DBBC3-2L2H (2 x 4GHz IF, 32 Gbps in 2-bit output mode)

DBBC3-4L4H (4 x 4GHz IF, 64 Gbps in 2-bit output mode)

DBBC3-6L6H (6 x 4GHz IF, 96 Gbps in 2-bit output mode)

DBBC3-8L8H (8 x 4GHz IF, 128 Gbps in 2-bit output mode)

The hardware supports a maximum of 512 Gbps in multi bit output mode

Firmware and software versions three phases:

PHASE 1:

1) ***DSC*** *mode*, input 4 GHz per IF, output 16 Gbps per IF, now operative

PHASE2:

1) ***FULL DDC*** *mode*, input 4 GHz per IF, output 128, 64, 32, 16, 8, 4, 2 MHz, 8 BBC/IF
   expected by beginning August 2017
2) ***OCT(opus) DDC***, input 4 GHz per IF, output 2048, 1024, 512, 256 MHz
   expected by end of summer 2017
3) ***DDC***, input 512, 1024 MHz per IF, output 128, 64, 32, 16, 8, 4, 2 MHz, DBBC2 compatibility
   expected by end of summer 2017

PHASE3:

1) ***FULL PFB*** *mode*, input 4 GHz per IF, output 256 MHz, expected by end 2017
2) ***PFB*** *mode*, input 512, 1024 MHz per IF, output 64, 32 MHz, DBBC2 compatibility
   expected by end of end 2017
3) ***DDC/PFB*** *mode*, input 4 GHz per IF, output 64, 32 MHz, tbd.
4) ***PFB/DDC*** *mode*, input 4 GHz per IF, output 128, 64, 32, 16, 8, 4, 2 MHz, tbd.

DBBC3 systems delivered and under construction:

APEX, DBBC3-4L4H

PICO VELETA, DBBC3-4L4H

HOBART, DBBC3-6L6H

YEBES, DBBC3-2L2H, GCoMO/CoMo

ONSALA1, DBBC3-8L8H

ONSALA2, DBBC3-8L8H

NyALESUND1, DBBC3-8L8H

NyALESUND2, DBBC3-8L8H

KATHERINE, DBBC3-6L6H

YARRAGDEE, DBBC3-6L6H

EFFELBERG, DBBC3-2L2H

KOREA, DBBC3-2L2H

red: delivered, black: under construction

News and new developments :

1) Sliced 10G -> disk module for CORE3H and FILA10G
2) ADB3H, full 14 GHz band sampler
3) New HAT-Lab web site
4) Web based maintenance support (experimental)