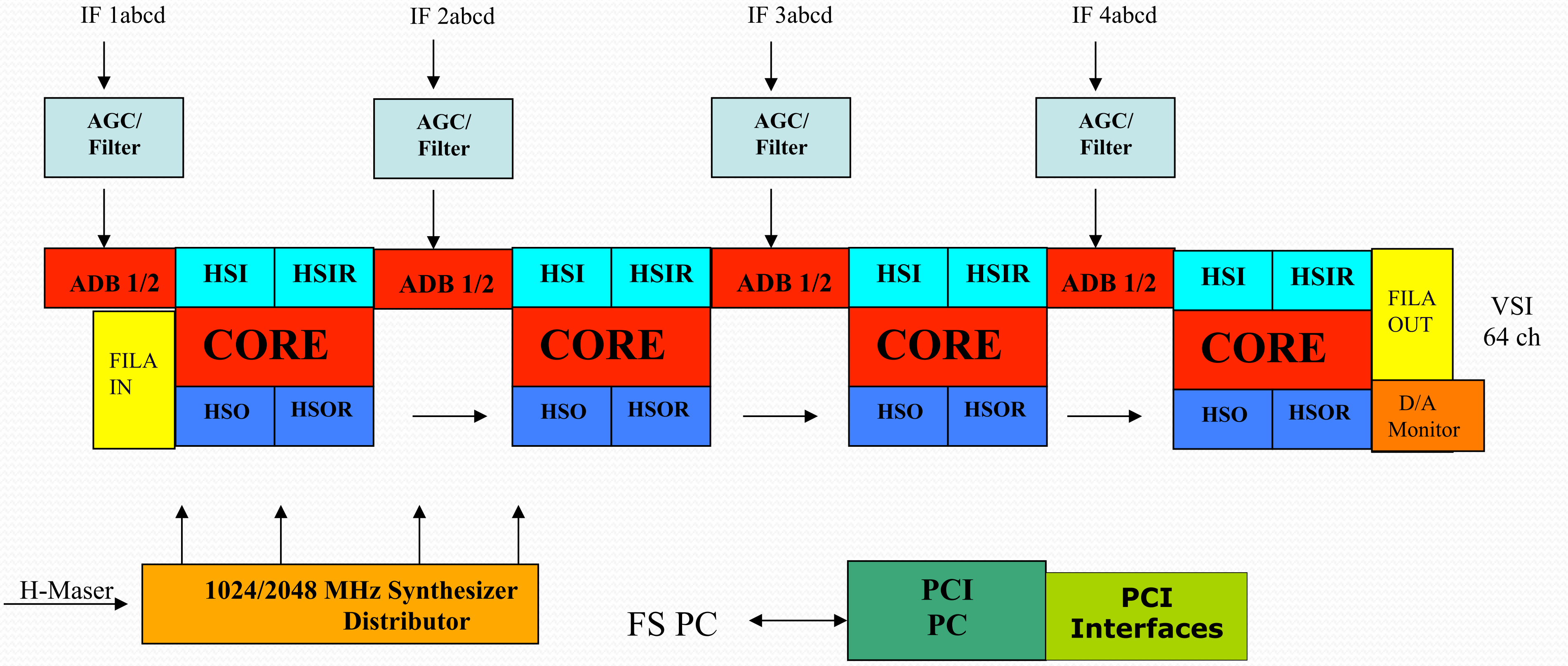
TOG Workshop
DBBC

Hardware Structure

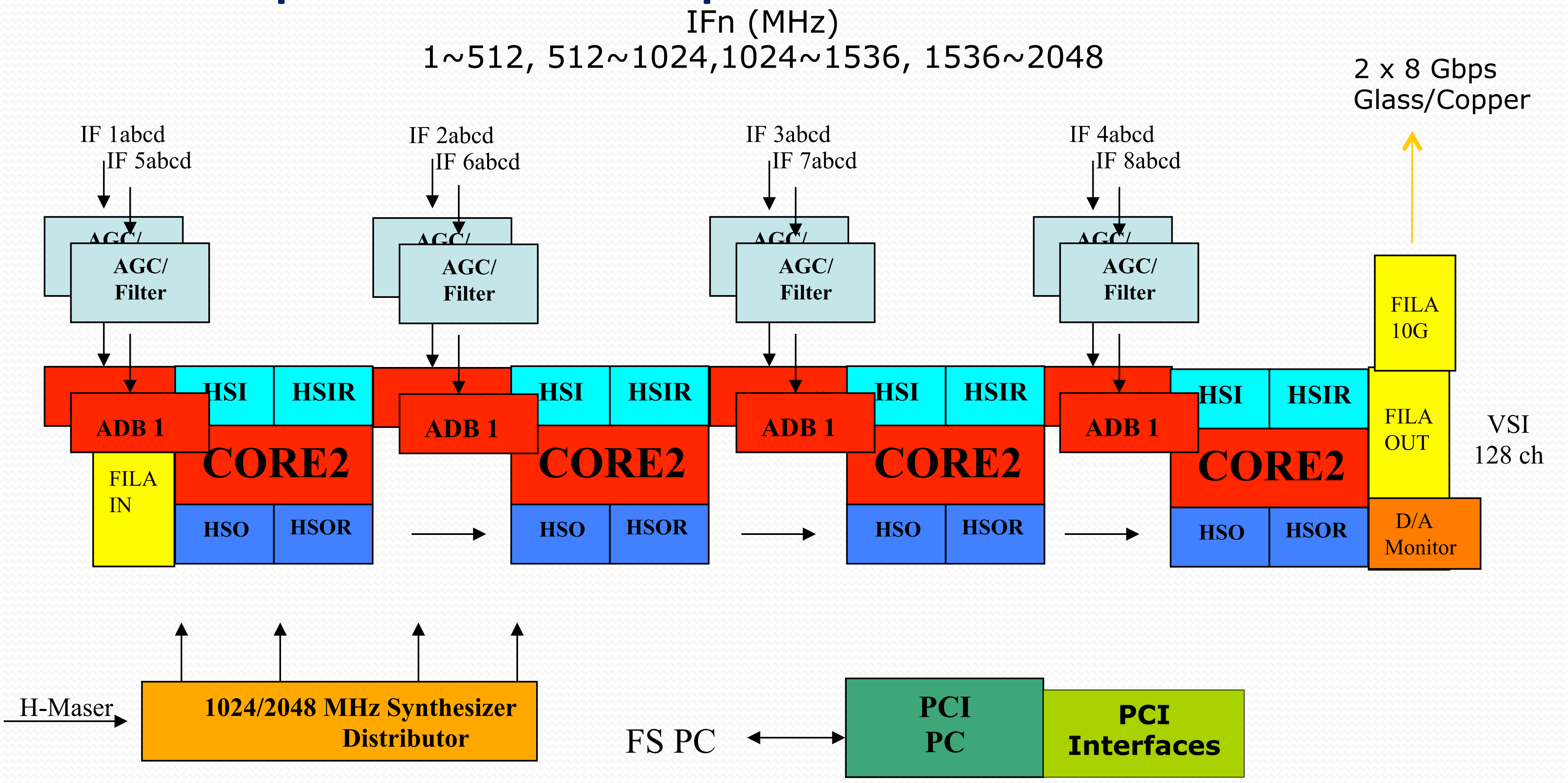
DBBC2 Architecture

IFn (MHz)
1~512, 512~1024,1024~1536, 1536~2048
or
1~1024, 1024~2048 MHz

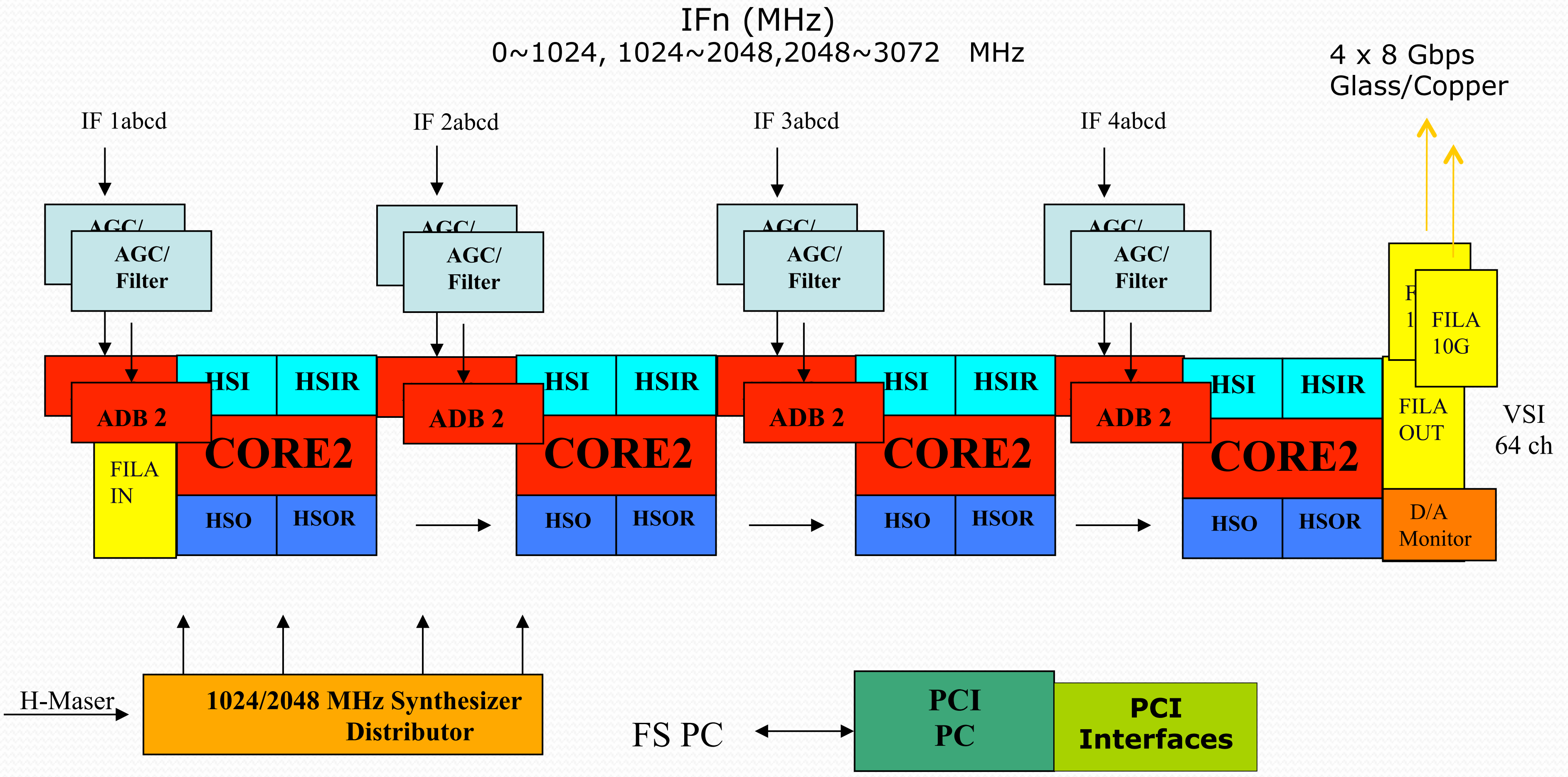


EVN TOG Workshop, Onsala 2012

DBBC2010 Architecture A
8 IFs @ 512 MHz
Output data rate 16 Gbps



DBBC2010 Architecture B
8 IFs @ 1024 MHz
Output data rate 32 Gbps



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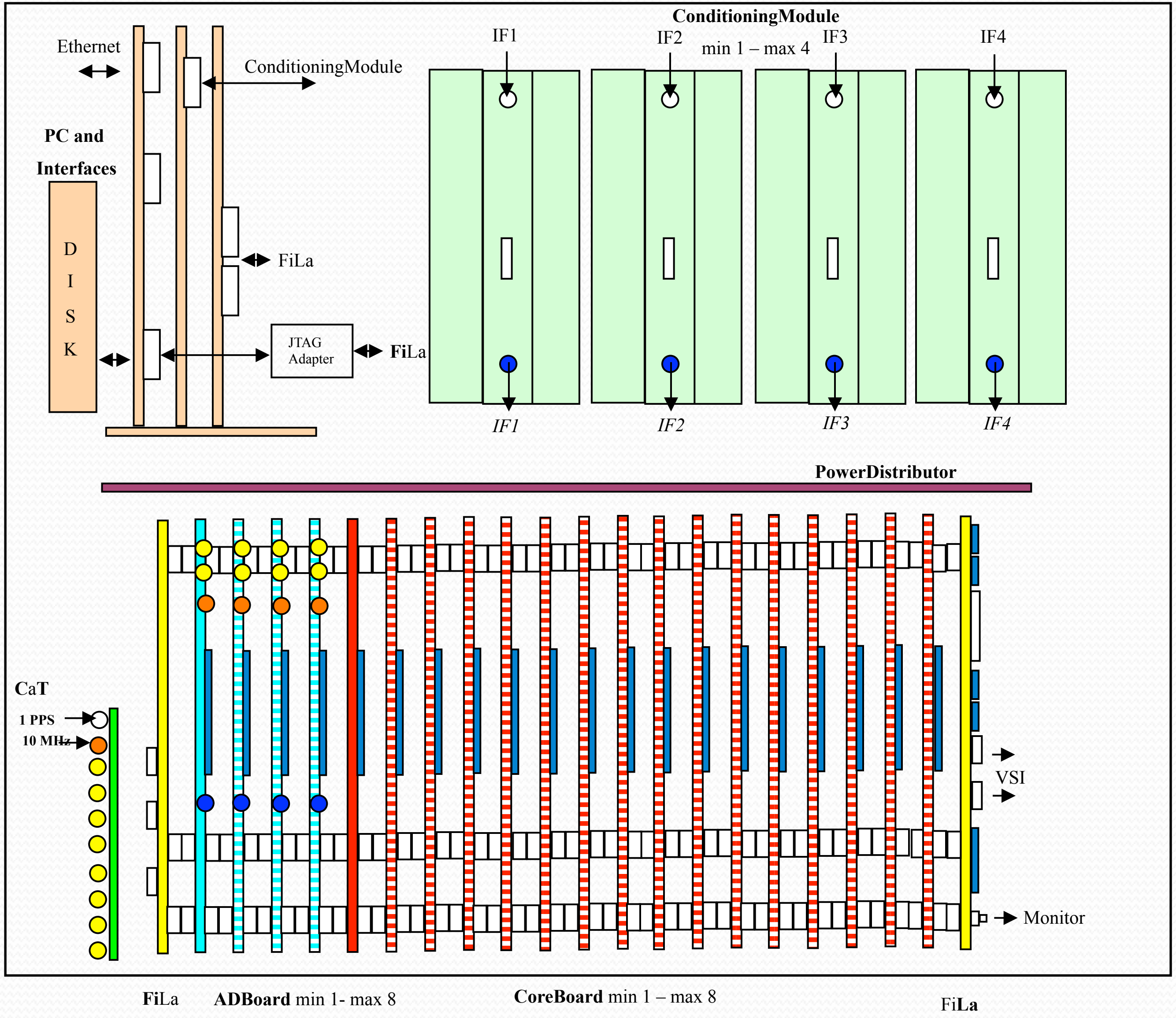
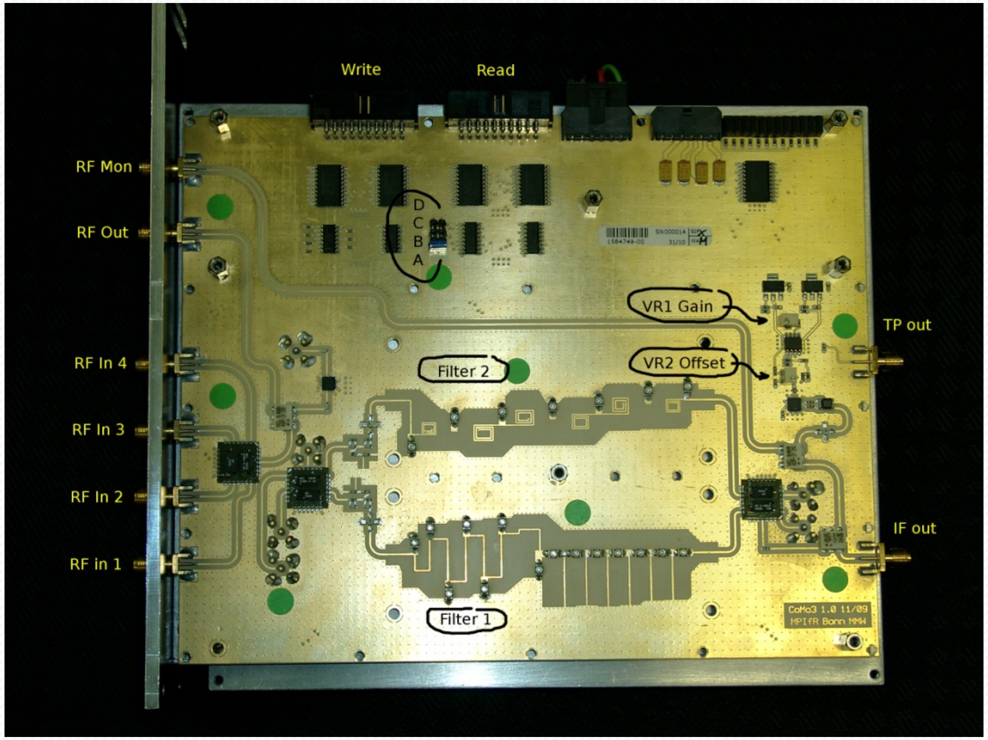
DBBC2
Schematic Top View



Review of the System Components

- Analog Conditioning Module
- Analog-Digital Converter (ADBoard1 - ADBoard2)
- Data Processing (CoreBoard2)
- Connection and Service (FiLaIN/OUT – FiLa10G)
- Timing and Clock (CaT1/2 – Clock and Timing Boards)
- Computer Control (PCSet)

Conditioning Module (Unica3)



4 selectable RF input

4 selectable Nyquist filters

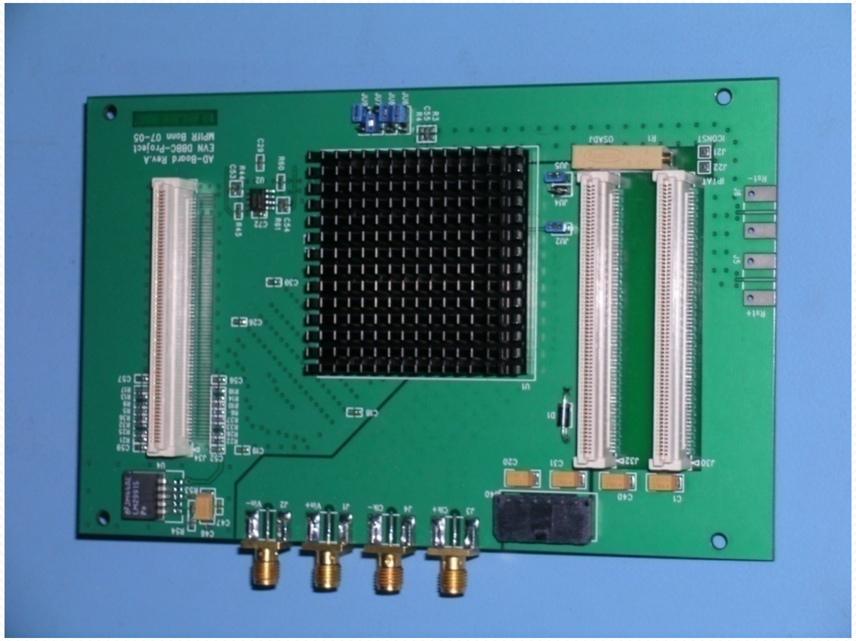
32 dB programmable attenuation

Total power full band

Manual or automatic gain control

ADBoard1

Analog to Digital Converter



Analog input: 0 - 2.2 GHz

Max Sampling clock single board: 1.5 GHz

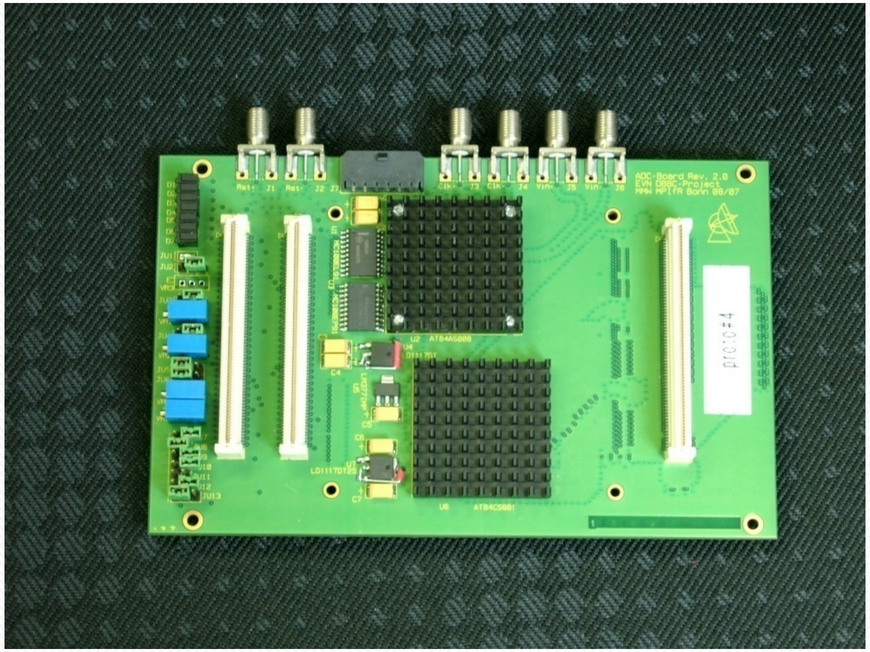
Max Istantaneous Bandwidth in Real Mode: 750 MHz

Max Istantaneous Bandwidth in Complex Mode: 1.5 GHz

Output Data: 2 x 8-bit @ ¼ SClk DDR

ADBoard2

Analog to Digital Converter



Analog input: 0 – 3.5 GHz

Max Sampling clock single board:
2.2 GHz

Max Istantaneous Bandwidth in Real Mode: 1.1 GHz

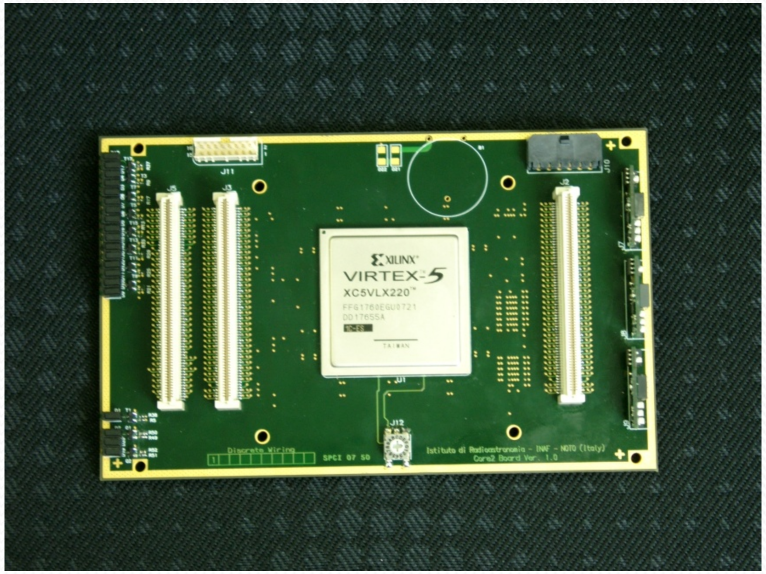
Max Istantaneous Bandwidth in Complex Mode: 2.2 GHz

Output Data: 2 x 8-bit @ ¼ SClk DDR
4 x 8-bit @ 1/8 SClk DDR

Piggy-back module support for 10-bit output and connection with FiLa10G board.

Core2

Basic processing unit



Input Rate:
(4 IFs x 2 bus x 8 bit x SClk/4 DDR) b/s
(2 IFs x 4 bus x 8 bit x SClk/8 DDR) b/s
More…

Typical Output Rate:
(64 ch x 32-64-128) Mb/s

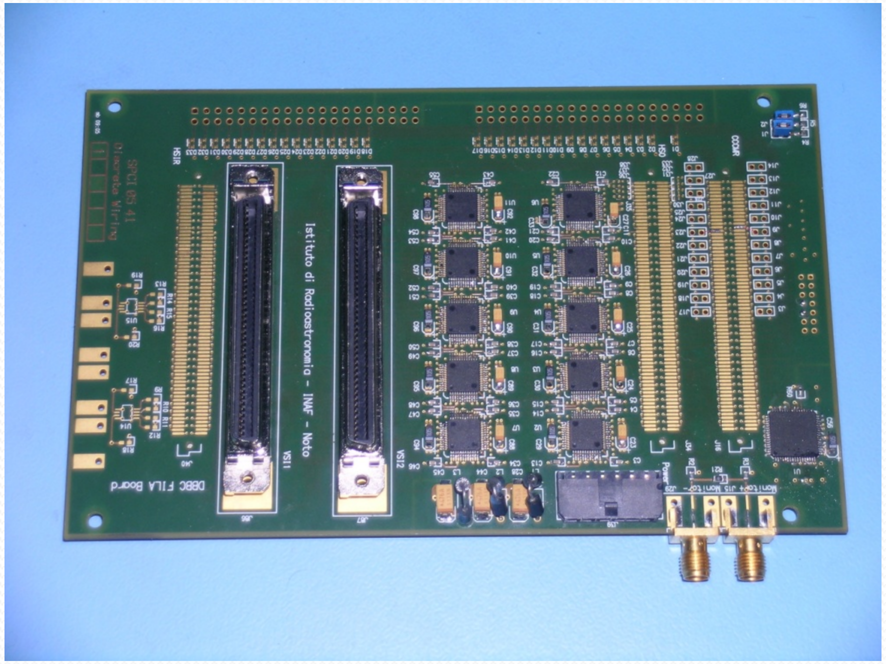
Programmable architecture

Es. Digital Down Converter:
1 CoreBoard2 = 4 BBC

Max Input/Output Data Rate 32.768 Gbps

FiLa Board

Connection and Service



First and Last board in the stack

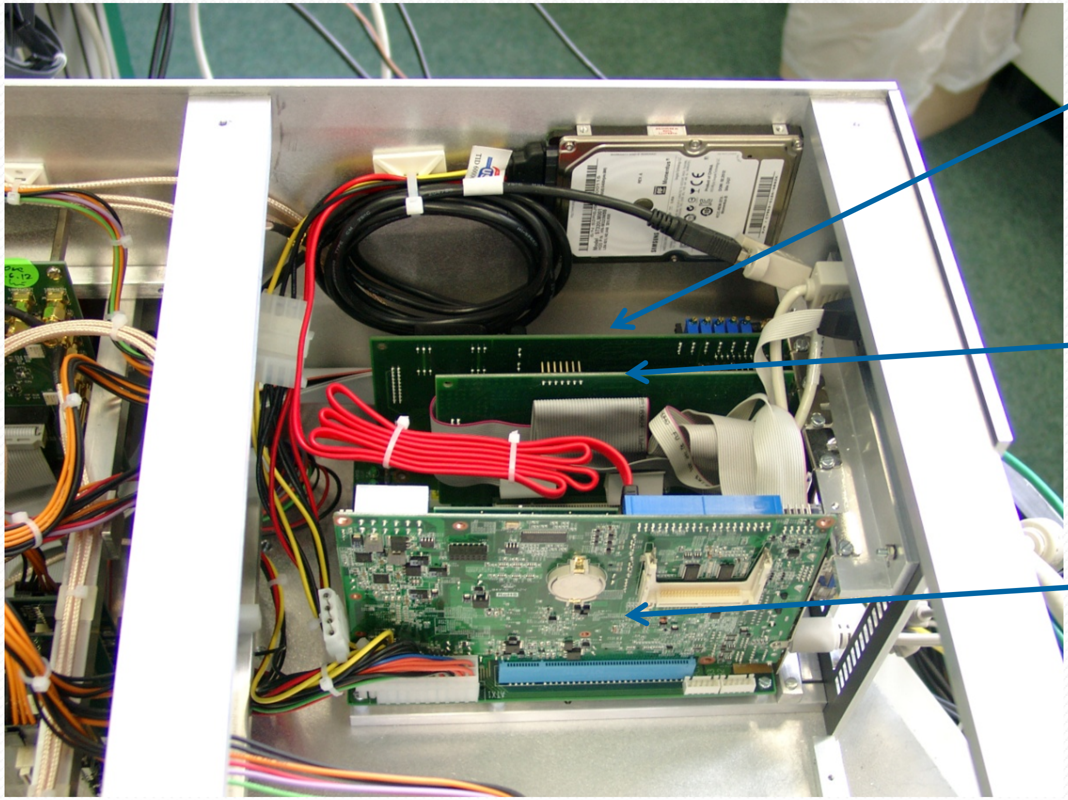
First:

Communication Interface
JTAG Programming Channel
1PPS Input

Last:

2 VSI Interfaces
DA Converter
1PPS Monitor Out
80Hz Continuous Cal Out

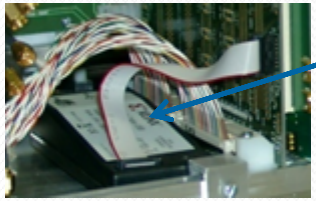
PCSet



ADLink PCI9111HR:
Communication with Conditioning Modules for IF total power measure, automatic gain control, registers control, etc.

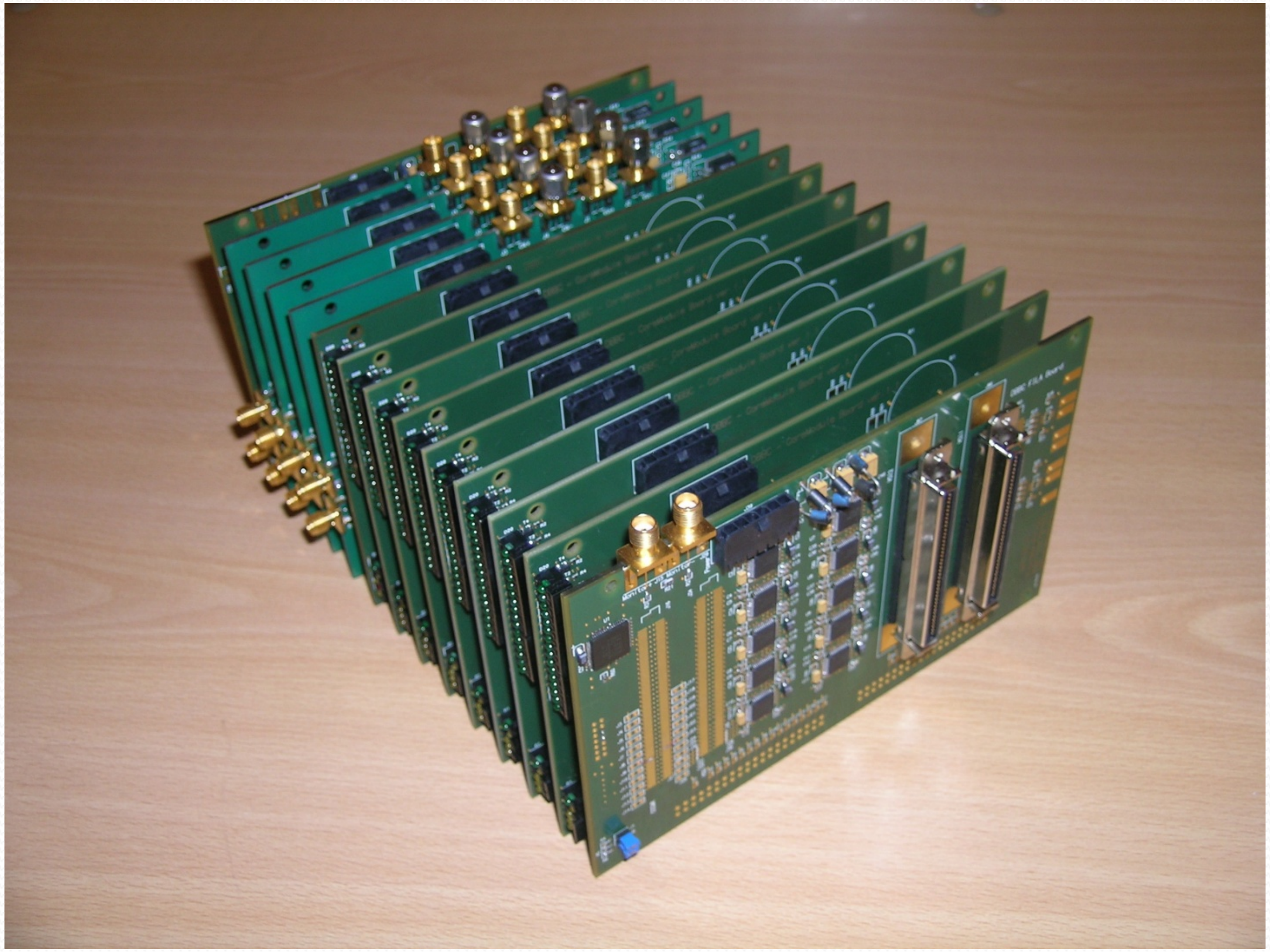
ADLink PCI7200:
Communication with 32-bit bus for Core2 register setting, total power measurement, state statistics, etc.

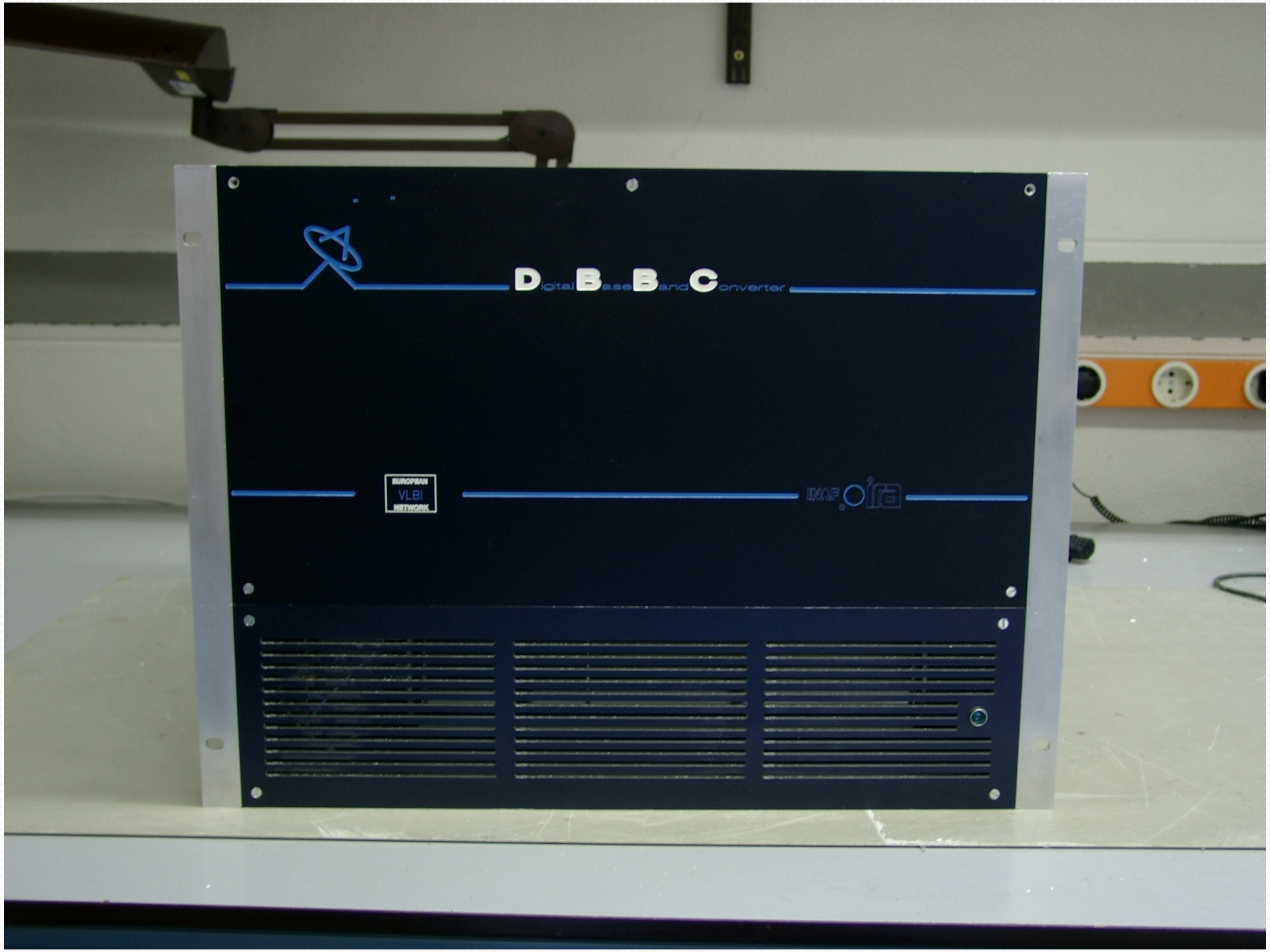
Adventech PCI-7030:
Half Size PCI Motherboard (Intel Atom) on PCI backplane

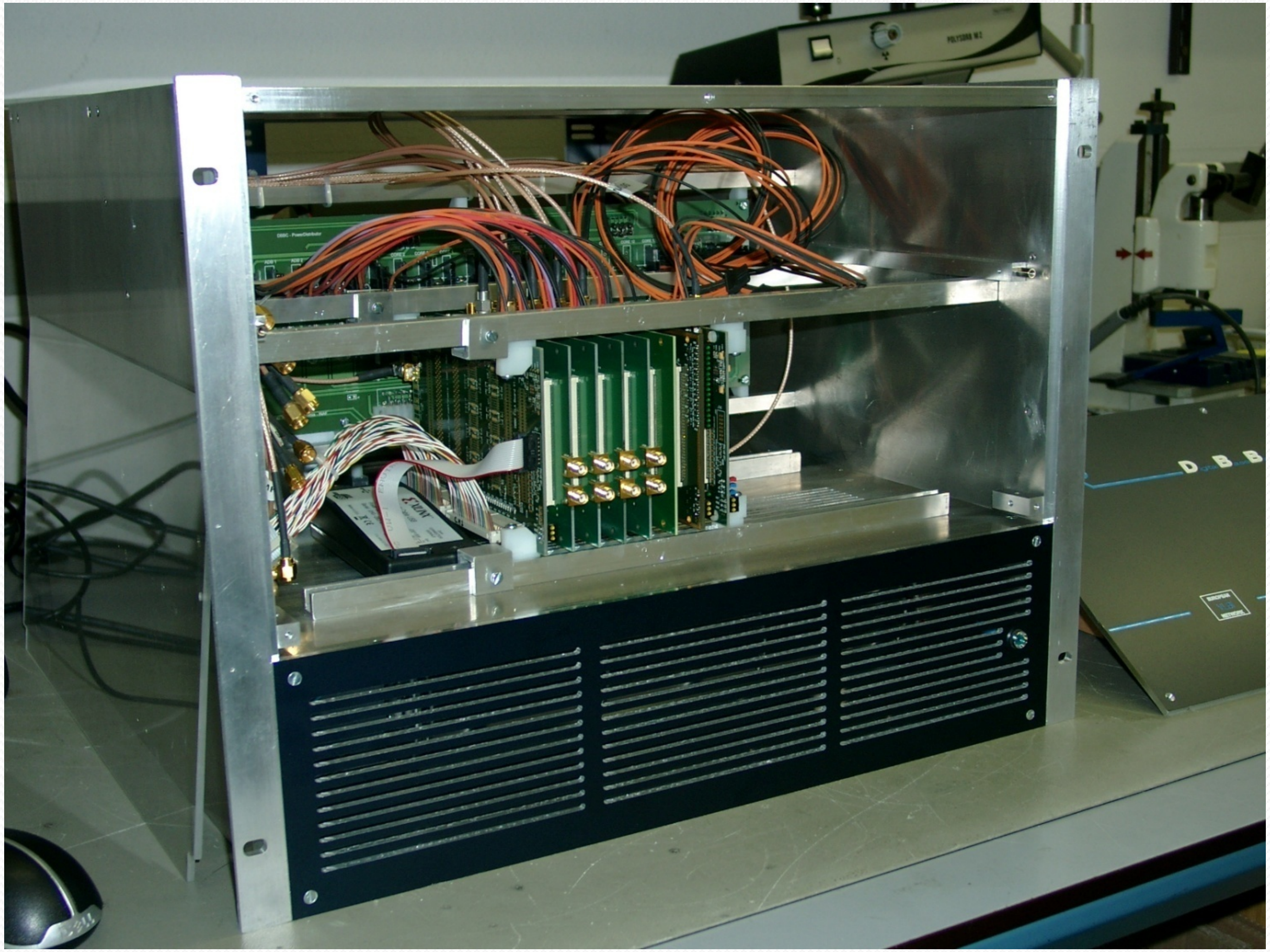


Xilinx programmer:
FPGA device configuration through USB – JTAG interface

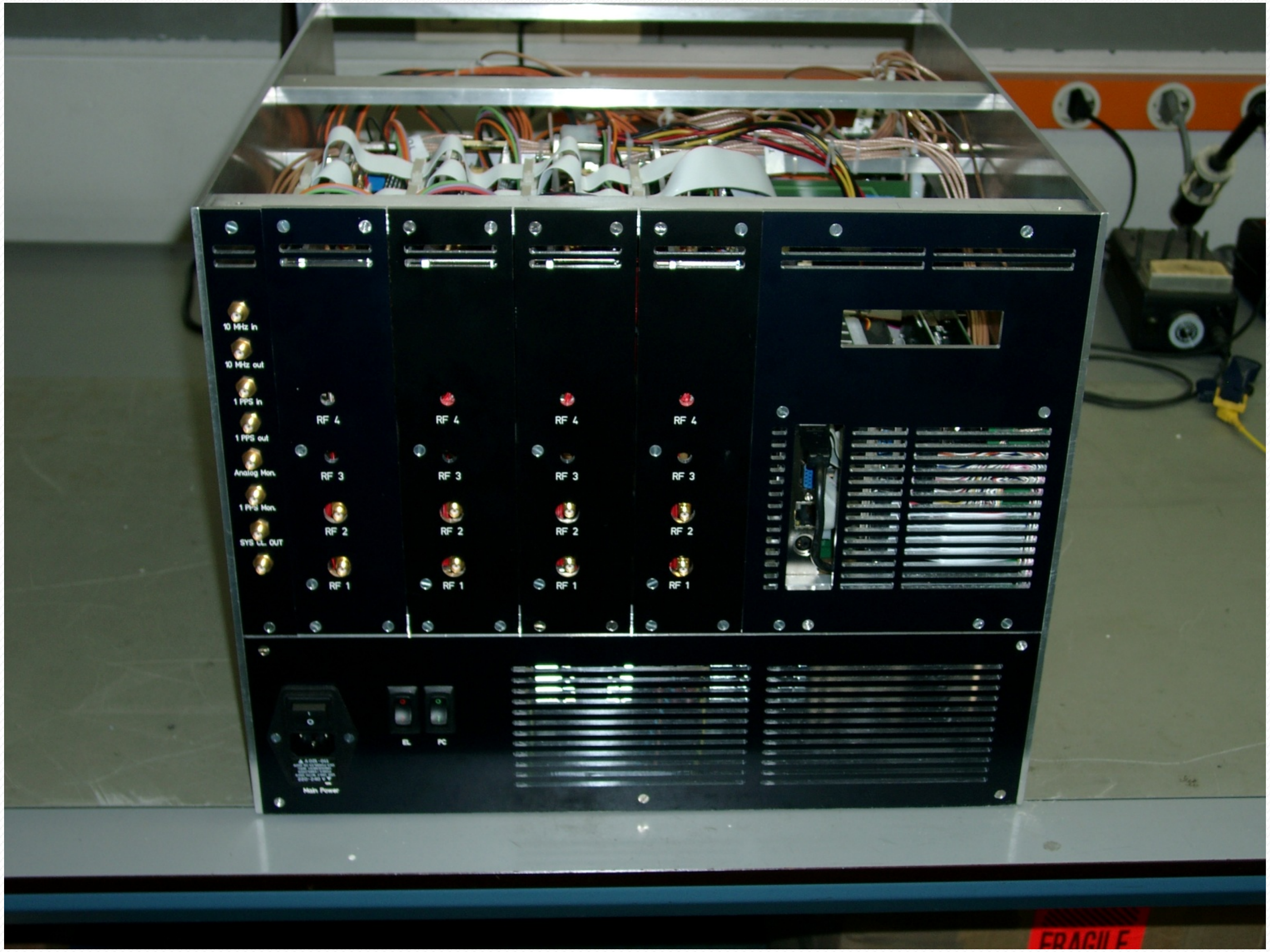
DBBC2 Module Stack



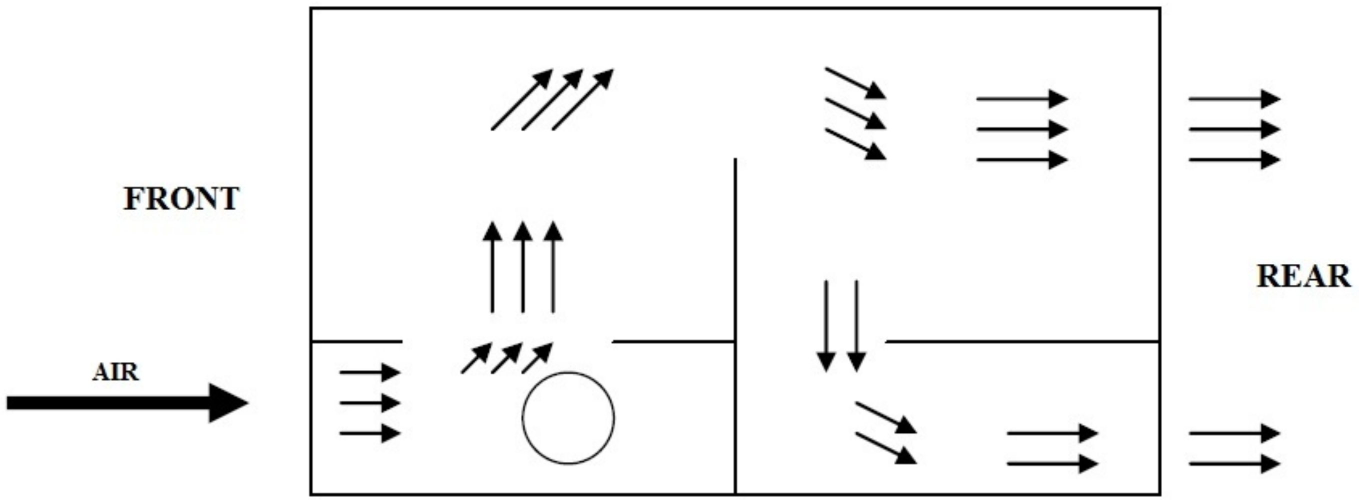

Digital Base Band Converter
EUROPEAN VLBI NETWORK
INAF ira



D B B

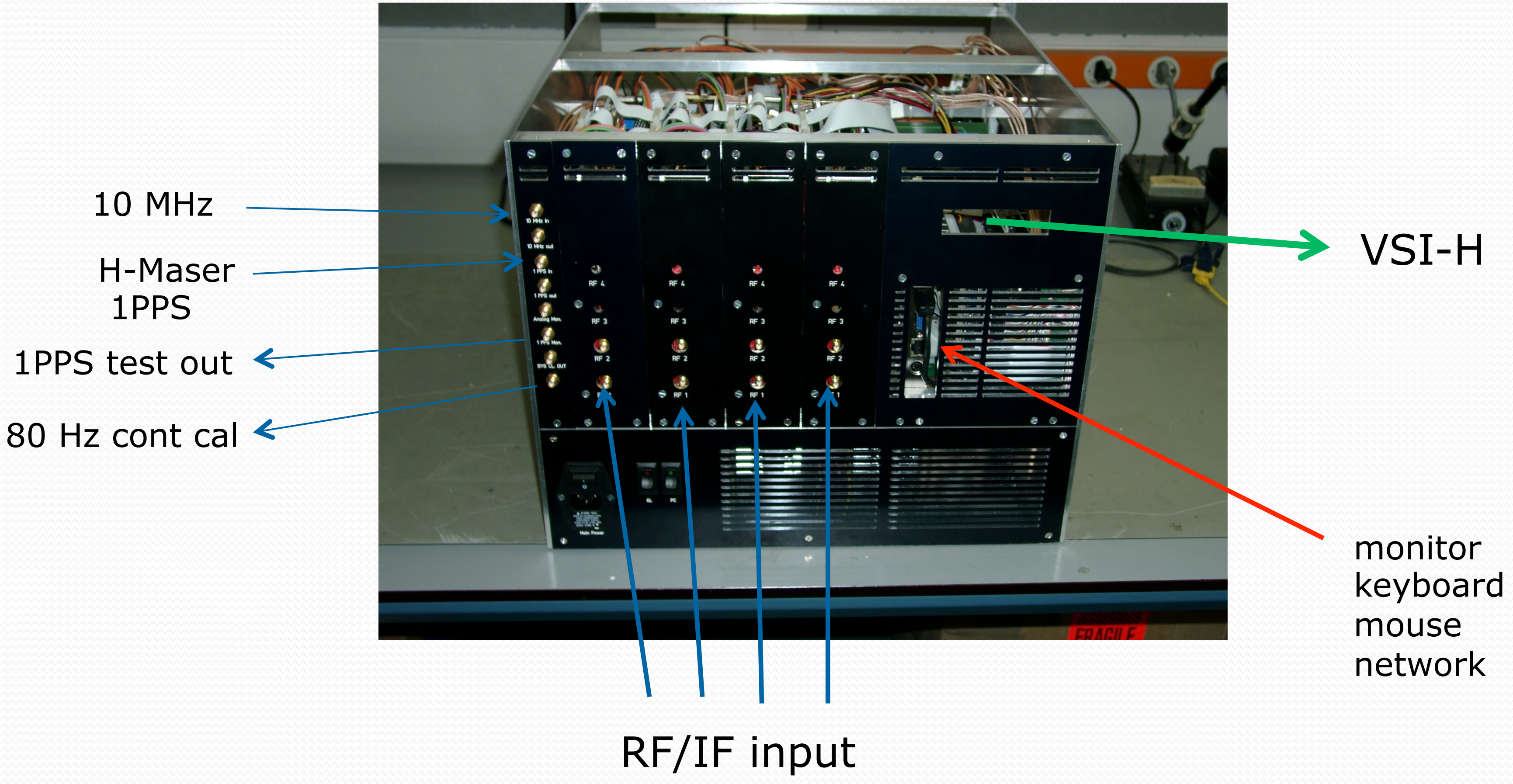

10 MHz in
10 MHz out
1 PPS in
1 PPS out
Analog Mon.
1 PPS Mon.
SYS CL. OUT
RF 4
RF 3
RF 2
RF 1
Main Power
EL
PC

DBBC Box: air-flow path



The air cooling flow from a side view

How the DBBC is to be connected in your control room



10 MHz

H-Maser 1PPS

1PPS test out

80 Hz cont cal

VSI-H

monitor
keyboard
mouse
network

RF/IF input

Observing Modes

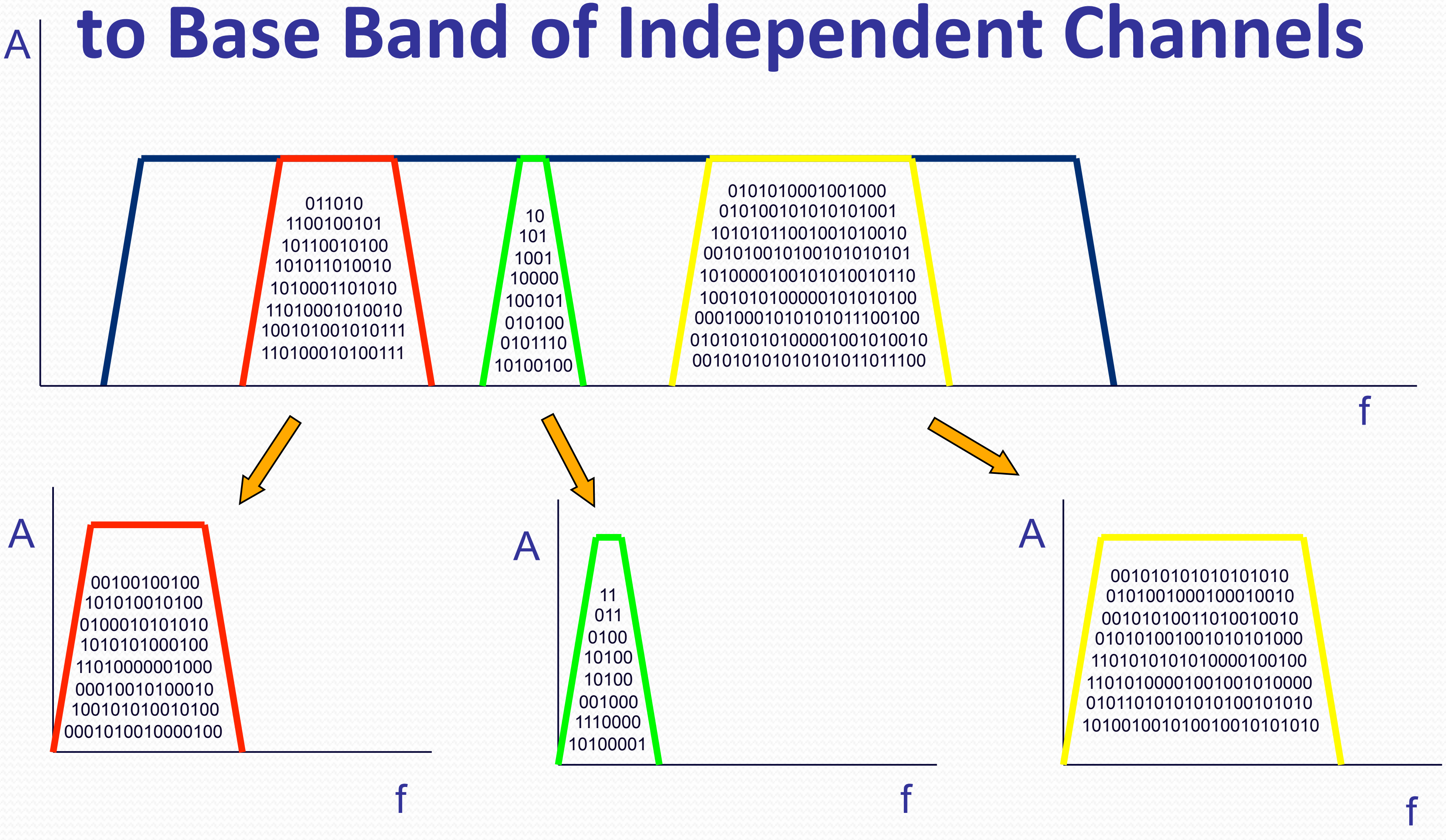
General Features (today)

- 4/8 RF/IF Input out of 16 (4x4) in a range up to 2.2 (3.5) GHz
- 1024/2048 MHz sampling clock frequency
- More personalities for more observing modes
- Four/eight polarizations or bands available in 4 groups of 32 output data channel, each group max 4 Gbps output data rate
- Output from the FILA OUT to FiLa10G Ethernet card max as 2 x 4 Gbps, 8 x 4 Gbps from Core2 piggy-back (ask if required)

Observing Modes (today)

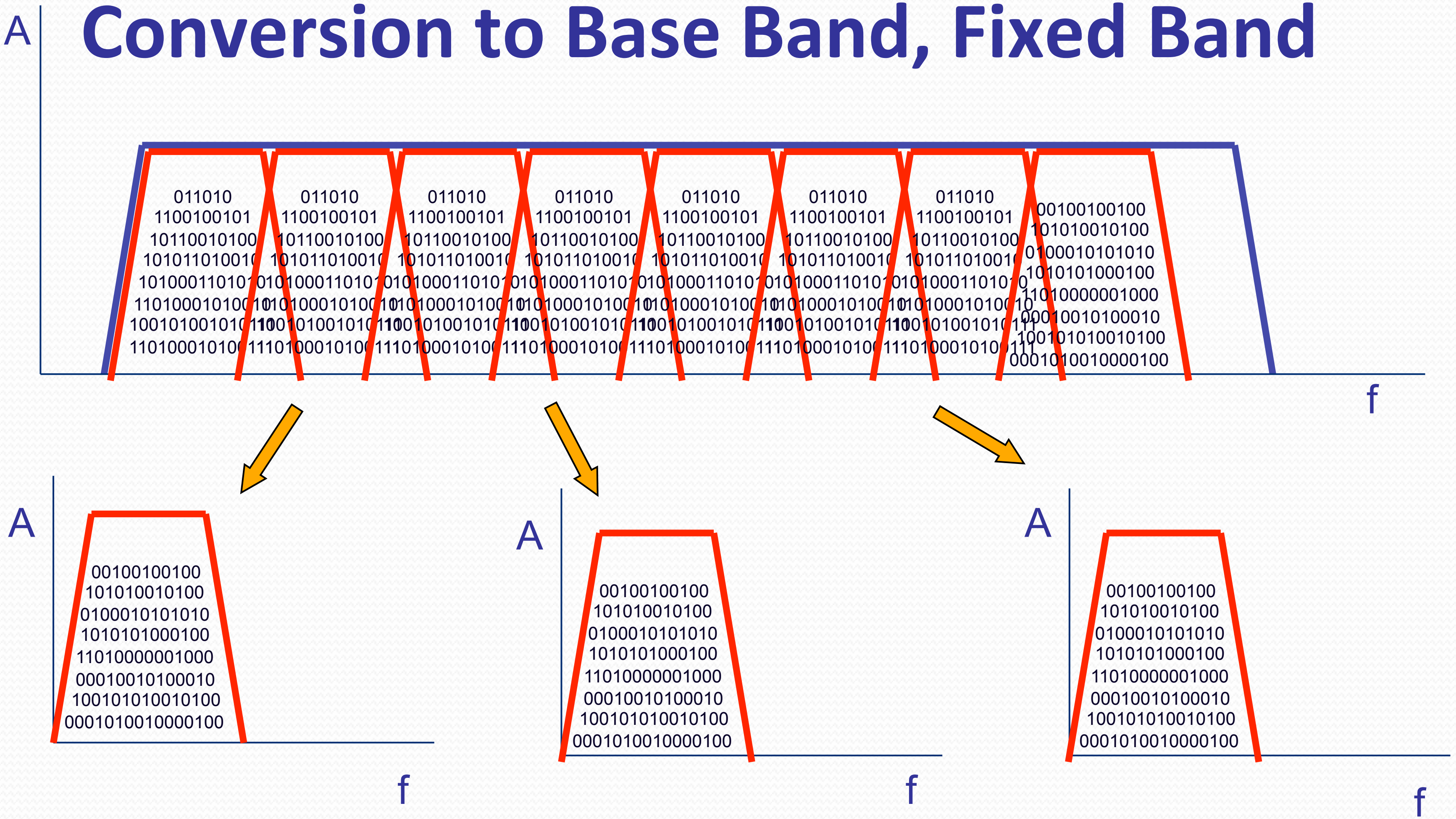
- **DDC**: tunable, channel bandwidth between 1 MHz and 16 MHz, U&L, Continuous cal with 80 Hz synchronization, mode ’astro’, ‘geo’, ‘w-astro’, ‘lba’, ’test’
- **PFB**: fixed tuning, channel bandwidth 32 MHz, all U or L depending on the Nyquist zone
- **DSC**: full 4 x 512 MHz , max 8 x 1024 MHz band direct sampling
- **SPECTRA**: 16K channels spectrometer

DDC - Digital Down Conversion to Base Band of Independent Channels

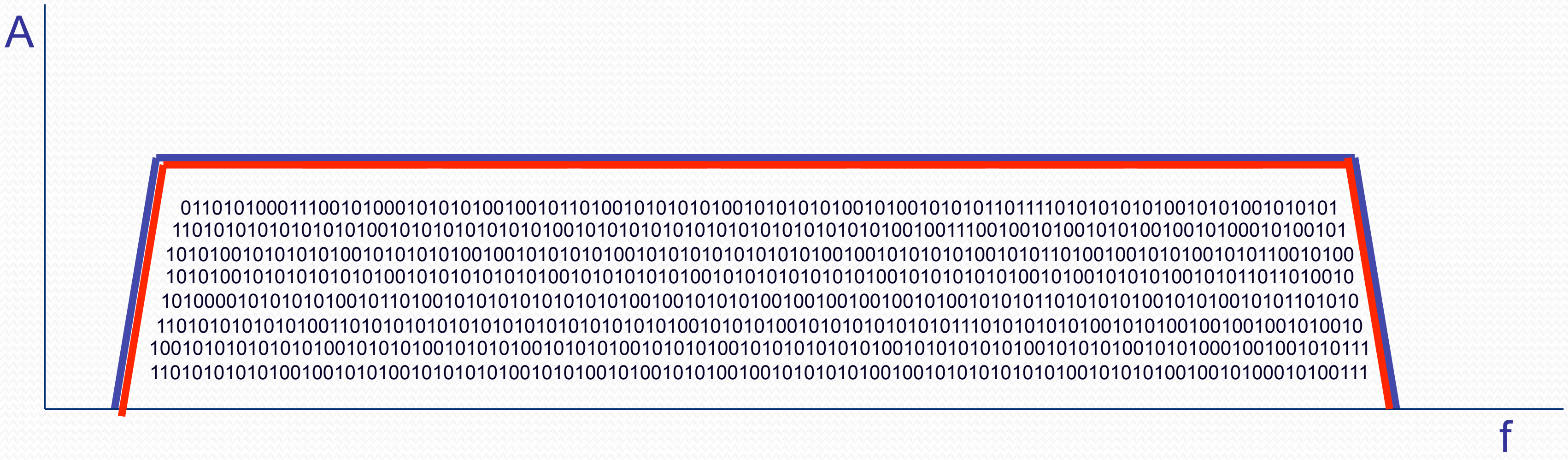


PFB – Polyphase Filter Bank

Conversion to Base Band, Fixed Band



DSC – Direct Single band Conversion
Conversion to Base Band, Full Band



How the observing mode is selected

- **Using a dedicated firmware**

- **Using a dedicated control software**

- **Using a dedicated configuration text file**

Software Structure

- **C:\DBBC\bin → control software**
- **C:\DBBC\doc → manuals**

- **C:\DBBC_CONF\ → configuration text files**
- **C:\DBBC_CONF\FilesDBBC → firmware**

Software

- **General:**

BASE Package

c:\DBBC\bin\clock1024.exe (CAT2 1024)
c:\DBBC\bin\clock2048.exe (CAT2 2048)
c:\DBBC\bin\ad9858.exe (CAT1)
c:\DBBC\bin\DBBC client v2.exe (general client)
c:\DBBC\bin\power.exe (on-off hardware)
c:\DBBC\bin\agc_if.exe (CoMo calibration)

DDC

Software on socket

- **DDC :**

c:\DBBC\bin\DBBC2 Control DDC v101.exe (server)

c:\DBBC_conf\dbbc_config_file_101.txt

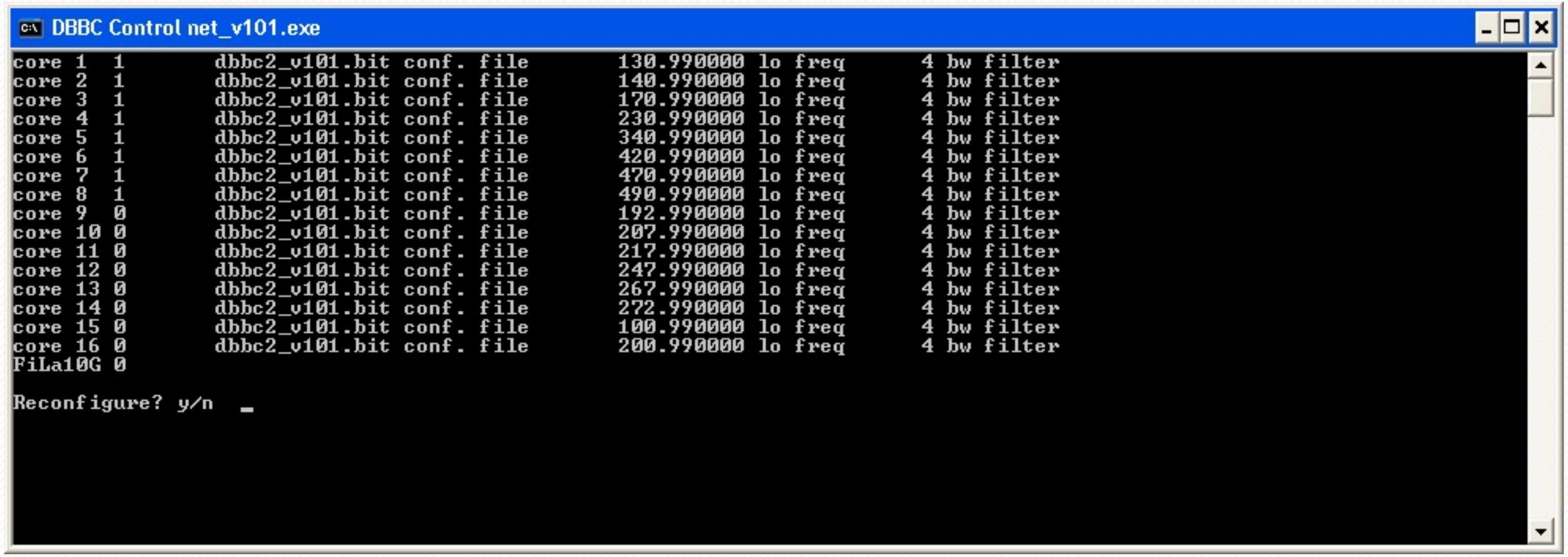
c:\DBBC_conf\FilesDBBC\dbbc2_ddc_v101.bit

c:\DBBC\doc\DBBC2 DDC command set v101.pdf

- c:\DBBC_conf\dbbc_config_file_101.txt

```
1 dbbc2_ddc_v101.bit 597.00 8
1 dbbc2_ddc_v101.bit 682.00 8
1 dbbc2_ddc_v101.bit 853.00 8
1 dbbc2_ddc_v101.bit 938.00 8
1 dbbc2_ddc_v101.bit 597.00 8
1 dbbc2_ddc_v101.bit 682.00 8
1 dbbc2_ddc_v101.bit 853.00 8
1 dbbc2_ddc_v101.bit 938.00 8
1 dbbc2_ddc_v101.bit 597.00 8
1 dbbc2_ddc_v101.bit 682.00 8
1 dbbc2_ddc_v101.bit 853.00 8
1 dbbc2_ddc_v101.bit 938.00 8
1 dbbc2_ddc_v101.bit 597.00 8
1 dbbc2_ddc_v101.bit 682.00 8
1 dbbc2_ddc_v101.bit 853.00 8
1 dbbc2_ddc_v101.bit 938.00 8
0 fila10g_v2.bit
38000 38000 38000 38000
100 100 100 100
CAT2 1024
```

DDC: running **DBBC2 Control DDC v101.exe**



```
core 1  1       dbbc2_v101.bit conf. file       130.990000 lo freq      4 bw filter
core 2  1       dbbc2_v101.bit conf. file       140.990000 lo freq      4 bw filter
core 3  1       dbbc2_v101.bit conf. file       170.990000 lo freq      4 bw filter
core 4  1       dbbc2_v101.bit conf. file       230.990000 lo freq      4 bw filter
core 5  1       dbbc2_v101.bit conf. file       340.990000 lo freq      4 bw filter
core 6  1       dbbc2_v101.bit conf. file       420.990000 lo freq      4 bw filter
core 7  1       dbbc2_v101.bit conf. file       470.990000 lo freq      4 bw filter
core 8  1       dbbc2_v101.bit conf. file       490.990000 lo freq      4 bw filter
core 9  0       dbbc2_v101.bit conf. file       192.990000 lo freq      4 bw filter
core 10 0       dbbc2_v101.bit conf. file       207.990000 lo freq      4 bw filter
core 11 0       dbbc2_v101.bit conf. file       217.990000 lo freq      4 bw filter
core 12 0       dbbc2_v101.bit conf. file       247.990000 lo freq      4 bw filter
core 13 0       dbbc2_v101.bit conf. file       267.990000 lo freq      4 bw filter
core 14 0       dbbc2_v101.bit conf. file       272.990000 lo freq      4 bw filter
core 15 0       dbbc2_v101.bit conf. file       100.990000 lo freq      4 bw filter
core 16 0       dbbc2_v101.bit conf. file       200.990000 lo freq      4 bw filter
FiLa10G 0

Reconfigure? y/n  _
```

after the Core2 configuration is completed

then run a client ex. **DBBC Client v2.exe or Field System**

DDC Mode Commands and Form Table (see documents)

DDC settings and optimization

- Phase optimization: to be performed with a synthesizer and the dedicated command at the system installation.

  To be repeated after a hardware modification in the stack or transportation. Periodically as a general check.
- Amplitude optimization: to be performed using phase cal tones injected in the receiver and 'bpcal' software from Haystack.

  To be repeated after a hardware modification, new receivers, etc. Periodically as a general check.
- Zero baseline with a second system if available, or intra-system at the installation and as a periodic check.

PFB

Software on socket

- **PFB :**

c:\DBBC\bin\ DBBC2 Control PFB v12_1.exe (server)

c:\DBBC_conf\ dbbc_poly_config_file_12.txt

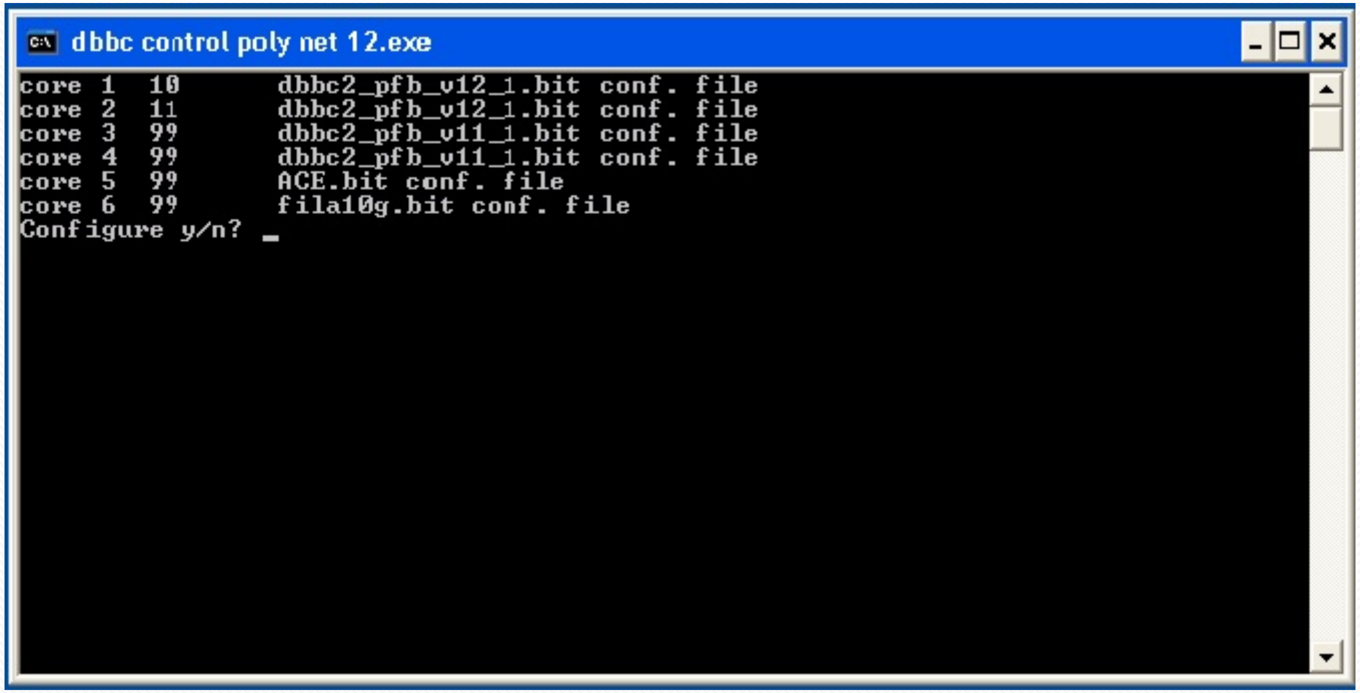
c:\DBBC_conf\FilesDBBC\ dbbc2_pfb_v12.bit

c:\DBBC\doc\ DBBC2 PFB command set v12.pdf

- **c:\DBBC_conf\ dbbc_poly_config_file_12.txt**

```
10 dbbc2_pfb_v12.bit
11 dbbc2_pfb_v12.bit
12 dbbc2_pfb_v12.bit
13 dbbc2_pfb_v12.bit
99 ACE.bit
99 fila10g_v2.bit
38000 38000 38000 38000
0 0 0 0
CAT2 1024
```

DDC: running **DBBC2 Control PFB v12_1.exe**



```
core 1  10      dbbc2_pfb_v12_1.bit conf. file
core 2  11      dbbc2_pfb_v12_1.bit conf. file
core 3  99      dbbc2_pfb_v11_1.bit conf. file
core 4  99      dbbc2_pfb_v11_1.bit conf. file
core 5  99      ACE.bit conf. file
core 6  99      fila10g.bit conf. file
Configure y/n? _
```

after the Core2 configuration is completed

then run a client ex. **DBBC Client v2.exe or Field System**

PFB Mode Commands, Form Table , PFB Frequencies (see documents)

PFB Full Flex with v13

- dbbcform= board, flex
- dbbcmap=board,*x0*,*x2*,….,*x15*

xn can be any Core2 local PFB (or HSOR) channel

PFB settings and optimization

- Phase optimization: to be performed with a synthesizer and the dedicated command at the system installation.

  Values are different by the DDC ones.

  To be repeated after a hardware modification in the stack or transportation. Periodically as a general check.
- Amplitude optimization: to be performed using phase cal tones injected in the receiver and 'bpcal' software from Haystack.

  To be repeated after a hardware modification, new receivers, etc. Periodically as a general check.
- Zero baseline with a second system if available, or intra-system at the installation and as a periodic check.

DSC

Software on socket

- **Implemented inside PFB software and firmware with 'dbbcmode=full', so again:**

c:\DBBC\bin\ DBBC2 Control PFB v12_1.exe (server)

c:\DBBC_conf\ dbbc_poly_config_file_12.txt

c:\DBBC_conf\FilesDBBC\ dbbc2_pfb_v12.bit

c:\DBBC\doc\ DBBC2 PFB command set v12.pdf

DSC settings and optimization

- Phase optimization: PFB recommendations
- Amplitude optimization: PFB recommendations
- Zero baseline with a second system if available, or intra-system at the installation and as a periodic check
- Dedicated test software developed and running on MK5B+

SPECTRA

Software on socket

- **SPECTRA :**

c:\DBBC\bin\ DBBC2 Control SPC v0.exe (server)

c:\DBBC_conf\ dbbc_spc_config_file_0.txt

c:\DBBC_conf\FilesDBBC\ dbbc2_spc_v0.bit

c:\DBBC\doc\ DBBC2 SPC command set v0.pdf

- **c:\DBBC_conf\ dbbc_spectra_config_file_0.txt**

```
10 dbbc2_spc_v0.bit
11 dbbc2_spc_v0.bit
12 dbbc2_spc_v0.bit
13 dbbc2_spc_v0.bit
99 ACE.bit
99 fila10g_v2.bit
38000 38000 38000 38000
0 0 0 0
CAT2 1024
```

Note: mixed SPECTRA and DDC/PFB mode is possible

Spectra Commands

- **exp_name=param1,[param2]** experiment name (used in the files produced)

param1	param2
experiment name	folder

- **int_time=param1** integration time

param1

integration time in milliseconds

- **spectrum=on,[param1]** start the acquisition ON-SOURCE

param1

on|off	noise source status

- **spectrum=off,[param1]** stop the acquisition OFF-SOURCE

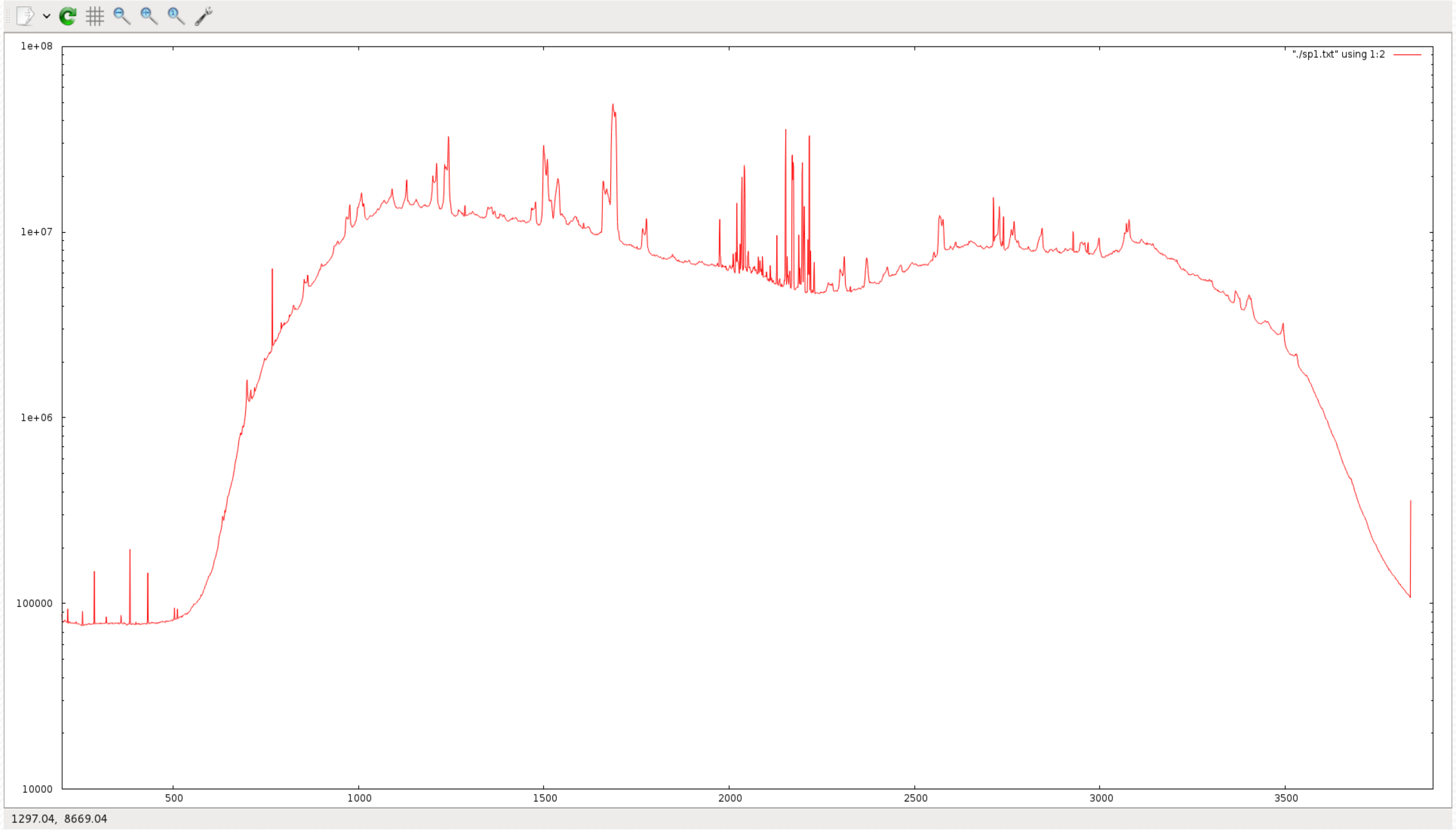
param1

on|off	noise source status

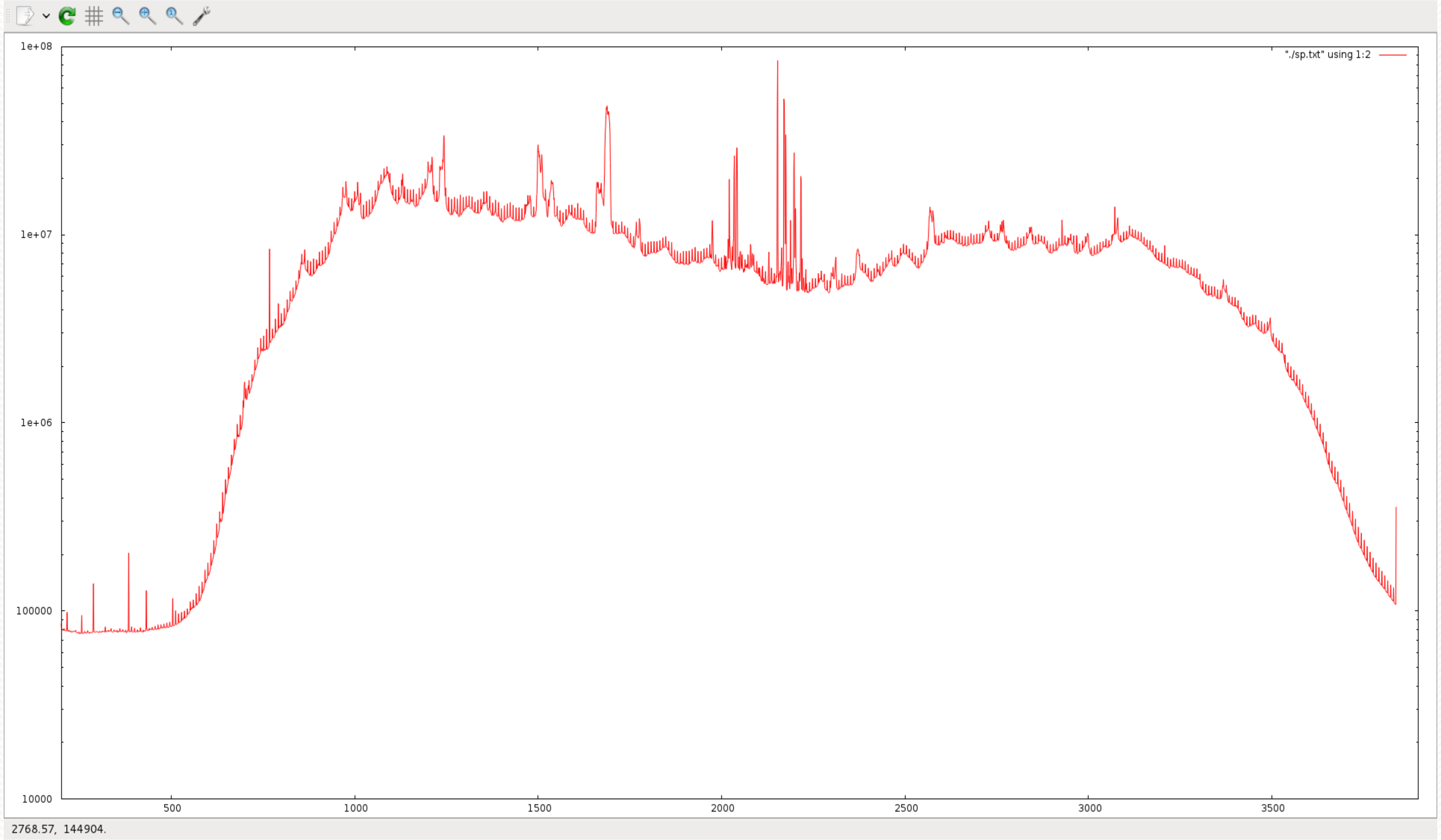
Spectra Commands (cont.)

dbbcifA|B|C|D	like DDC/PFB
pps_sync	like DDC/PFB
phase	like DDC/PFB
calibration	like DDC/PFB

Noto L band cal tones off



Noto L band cal tones on



Other Observing Modes under way?

- **512 MHz DDC tunable 32MHz bwd**
- **1024 MHz DDC tunable 32MHz bwd**
- **1 GHz Polyphase Filter Bank (16 ch x 64 MHz bwd)**
- **Spectro-polarimeter**

FiLa10G

10G Optical Fiber Ethernet Board

- Triangle connection between HSI (DBBC fast sampled data bus) – VSI – 10Gb link

- It can be placed either at the beginning or at the end of the stack chain → 10G link / MK5C

- Piggy-back board for ADB2

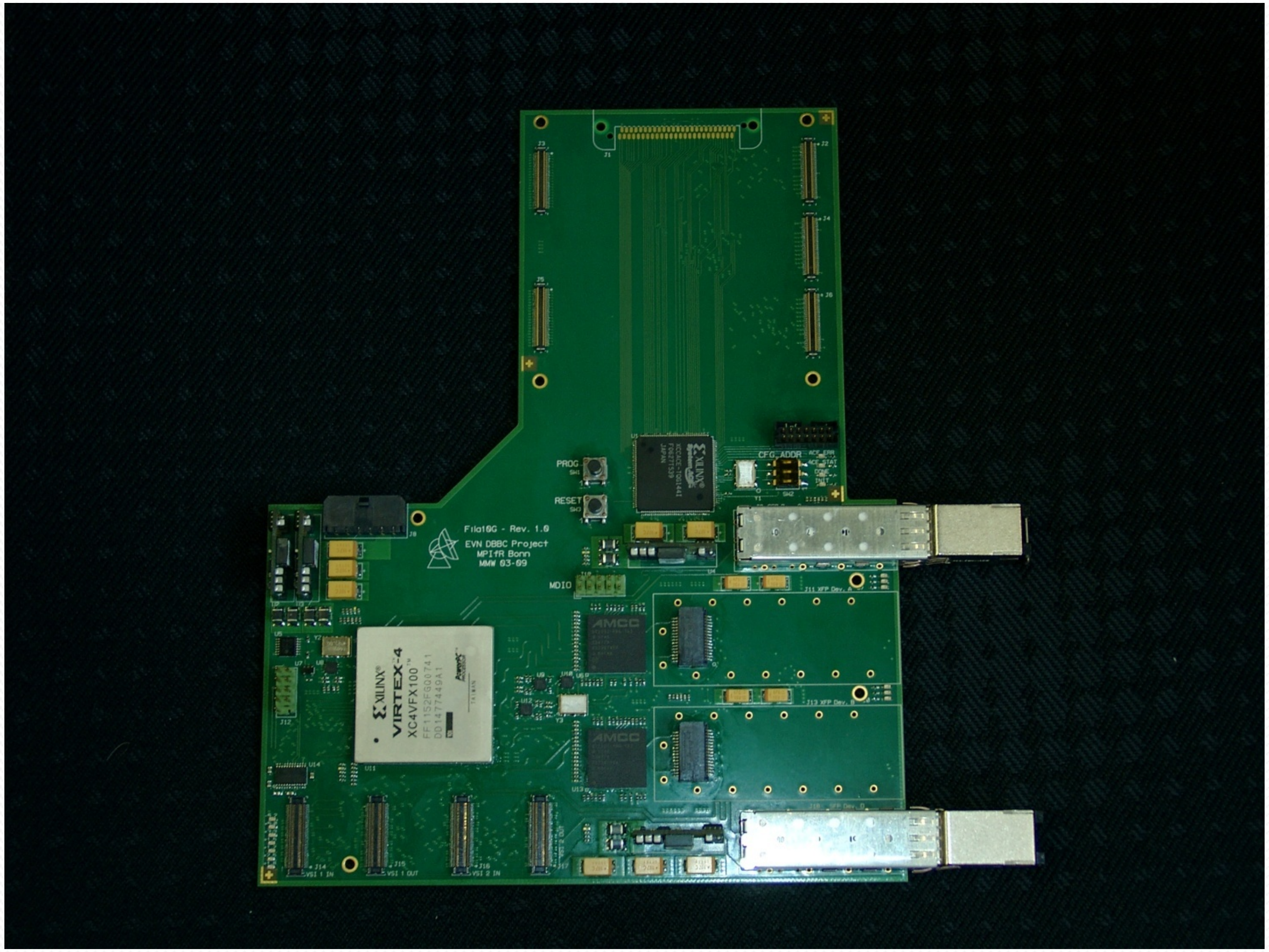
FILA10G main features

- Two independent 10G Ethernet UDP port
- Physical interface optical XFP
- 10G port fully bidirectional
- Installed inside the DBBC box or as stand-alone
- Data rate: 1 – 2 – 4 – 8 Gbps each 10G port
- Format mode: MK5B in two 5008 bytes packets

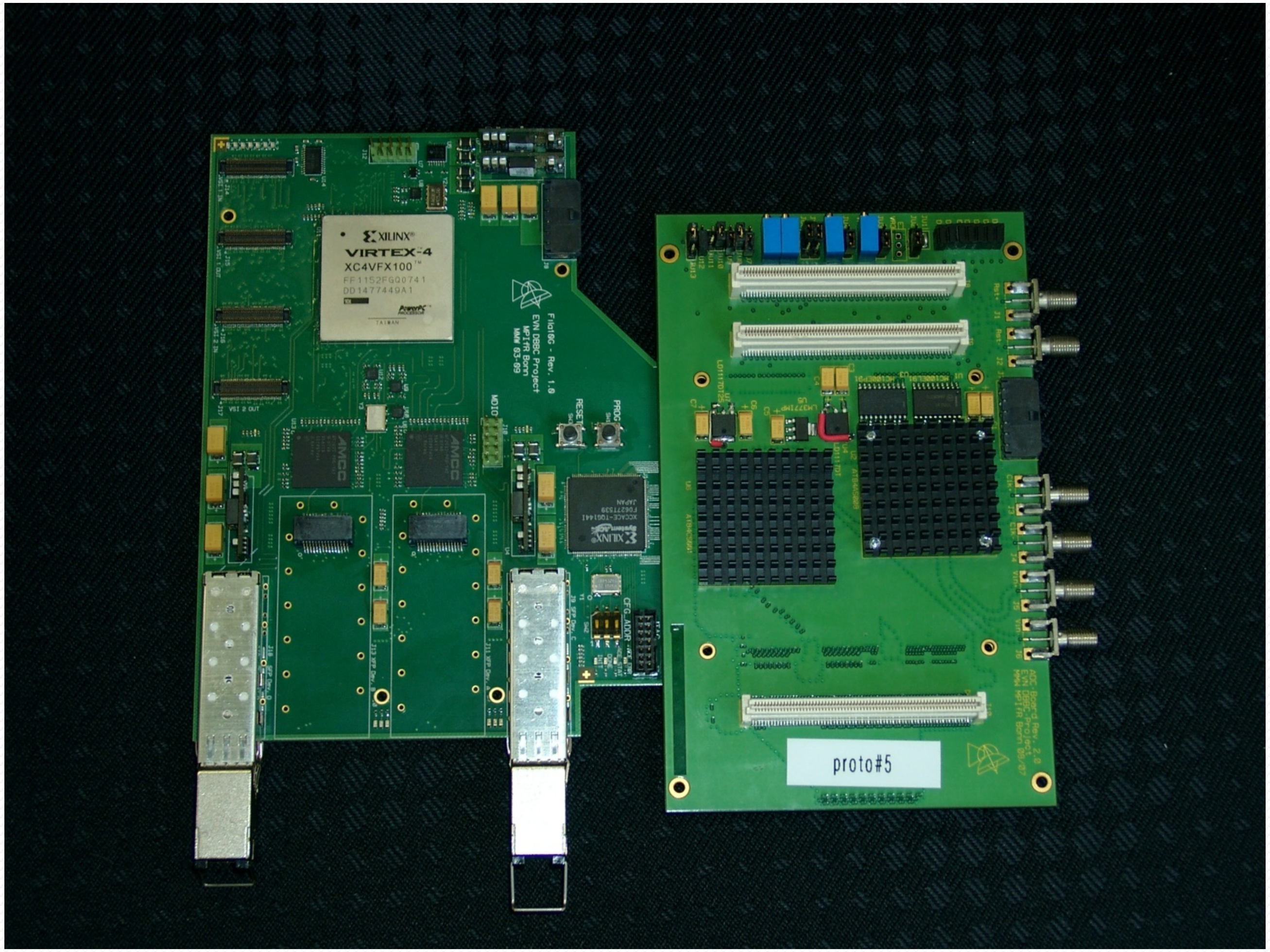
  VDIF-ST in any allowed packet size

  VDIF-MT corner turned under development

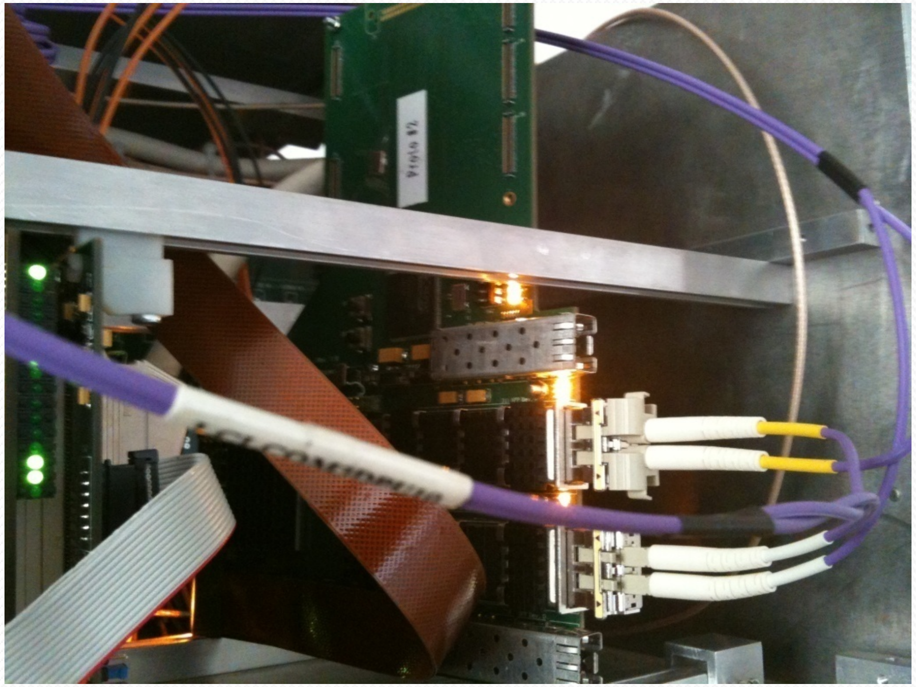
FILA10G

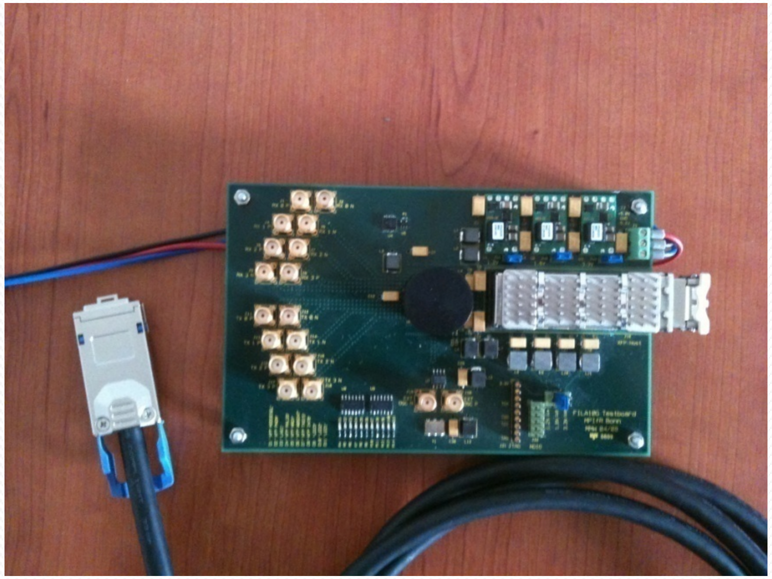

PROG
RESET
CFG_ADDR
Fila10G - Rev. 1.0
EVN DBBC Project
MPIfR Bonn
MMW 03-09
MDIO
XILINX
VIRTEX-4
XC4VFX100
AMCC
AMCC

FILA10G and ADB2

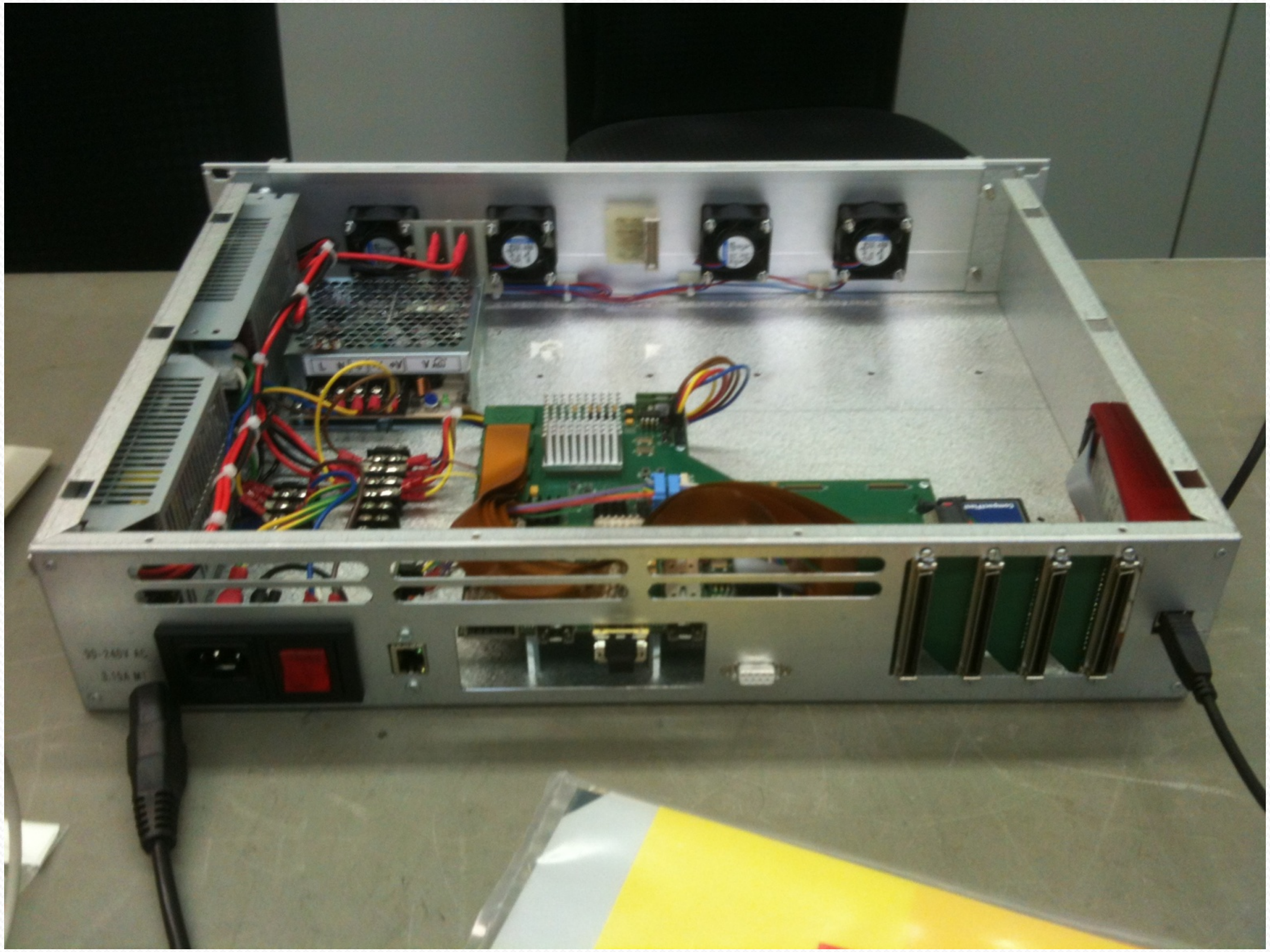


FILA10G and GLAPPER



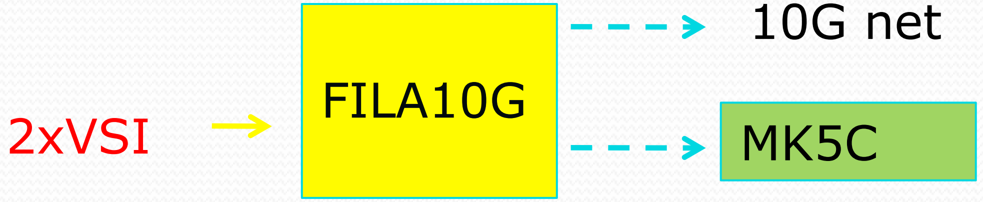


FILA10G - SA

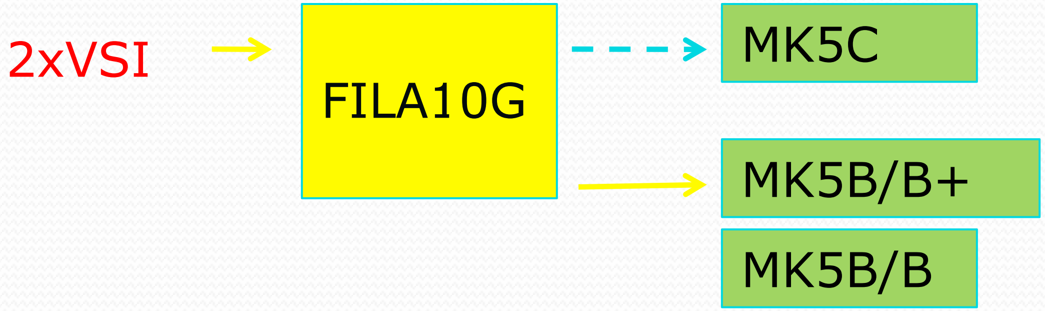


Connection examples

- 2 x VSI --> MK5C & 10GE net

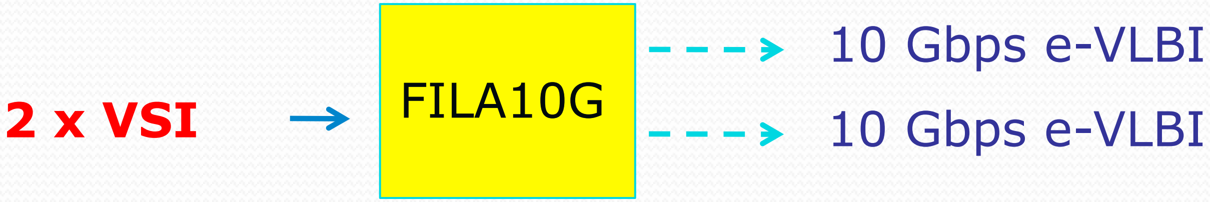


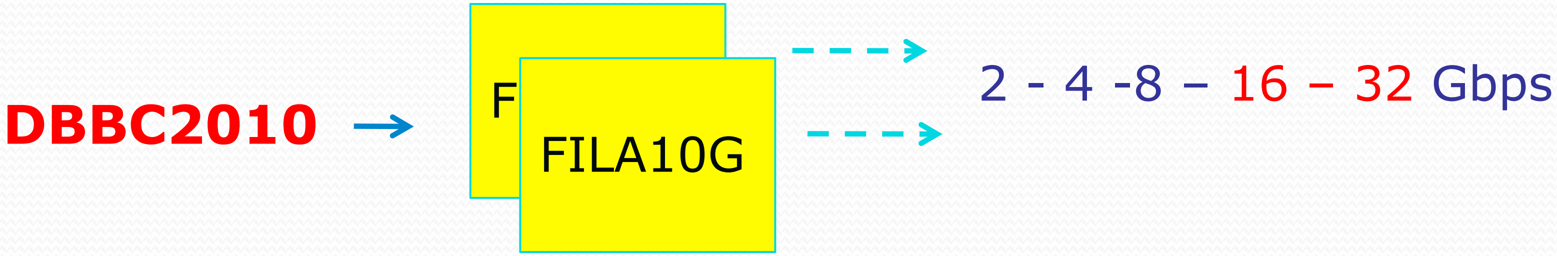
- 2 x VSI --> MK5C & MK5B



Connection examples

- 2 x VSI --> Network





How to set the FILA10G

- Download the firmware is automatically made by the DDC/PFB control software
- In the FILA-SA a script file can be used with the additional included Xilinx Jtag programmer
- Communication is through serial port or Ethernet in the stand-alone version
- Commands available (see document)
- VDIF packet size (see document)
- Script files can be used for block of commands (see example)

- **FILA10G Files:**

c:\DBBC\bin\ timesyncFILA10G.exe (MK5B time set)

c:\DBBC\bin\ vdif_timesyncFILA10G.exe (VDIF time set)

c:\DBBC\bin\ sendstr.exe (serial communication)

c:\DBBC_conf\FilesDBBC\ fila10g_v2.bit

c:\DBBC\doc\ DBBC2 FILA10G Command set v2.pdf

Note: a program to sync with a NTP server is required
(ex. NetTimeSetup-314.exe)

Commands integrated in DDC and PFB software

- **Fila10g=mode,param1,param2,param3** Data Format Mode

param1	param2	param3
5B	VSI1	VDIF packet size
VDIF-ST	VSI2	
	VSI1-2	
	TEST-2|4|8-0	
	TEST-2|4|8-1	
	TEST-2|4|8-bin	
	TEST-2|4|8-tvg	

- **Fila10g=synch,param1,[param2],[param3]**

param1	param2[5B]	param3[5B]	param2[VDIF]	param3[VDIF]
5B	MJD	sec	semfrom2K	sec
VDIF				

if param2 and param3 are not indicated use of PC clock

- **Fila10g=start|stop** start or stop packet sending

- **Fila10g=direct,param1** direct transfer

param1

string to send