DBBC2 news

- **New PFB v16 (released in beta version)**
- **New DDC v106 and v106E (alpha version under test)**

PFB v16: novelties

- **‘FULL AUTO’** mode in ‘DBBCFORM’ for full band mode with magnitude automatically controlled

- **‘CONT_CAL’** command for continuous noise cal settings

‘POWER_CONT’ command for continuous TP measurements

- **‘CALIB_VSI’** command for optimize the intra-stack data output propagation

- **‘PCAL_DETECT’** for phase cal tone measurements

- **‘STAT_COUNT’** for statistics of the states measurements

- **Post frequency conversion detector** selection for the Conditioning Modules AGC control (not just the default)

‘FULL AUTO’

- **dbbcform** = form,[test_mode]

Set the output format:
form = spol => single pol output
form=dpolc => dual pol contiguous
form=dpolm => dual pol mirror
form=dpoli => dual pol interleaved
form=full => full band
form=full auto => full band with magnitude automatically controlled
form=byp => bypass
form=full => flex
form= copy => copy VSI1 on VSI2
form=test,0 => test mode all 0
form=test,0 => test mode all 1
form=test,bin => test mode binary counter
form=test,tvg => test mode TVG

‘CONT_CAL’

- **cont_cal** = status, freq, option
- Continuous calibration for noise diode activation.
- status => on|off, freq, option
- freq => rate of noise diode switching (in a range of about 8Hz - 300KHz)
- option => 2 = output always ON, 5 = inverted polarity
  - 2: can use for standard TSYS
  - 5: accomodate different hardware

‘POWER_CONT’

- **power_cont** = nn

total power reading for a bank of 15 adjacent channels as produced by a single Core2 on ON and OFF continuous noise cal

Additionally as **channel 0** is reported the total power of the full input band

nn => 1, .. ,4 indicates the board number for the client, while in the server window all the data is represented

Reports the total power values for all the bbcs in a PFB and as last indication a flag (0|1) for a **possible overflow status** (1) in the channels group

‘CALIB_VSI’

- **calib_vsi**

Start VSI phase calibration process and create output file in
C:\YYYY-doyTHHMMSS-calib_vsi_poly.txt

(technical note with description)

Note: technical description under preparation; similar to standard DBBC calibration

‘PCAL_DETECT’

- **pcal_detect** = board#, ch#, freq

board# => Core2 board to be set

ch# => local VSI1 output channel to check

freq => phase cal tone frequency to check

Reports: pcal_detect = board#, ch#, freq, amplitude, phase.
Amplitude and phase are related to the channel examined at the selected frequency.

‘STAT_COUNT’

- **stat_count** = board#, ch#

board# => Core2 board to be set

ch# => local VSI output channel to check

Reports: stat_count = nn, mm, stat

Where stat is in percentage the statistics status of the selected channel.

In the range 0-31 even channels (sign bit) should present values close to 48-52%,
odd channels (magnitude bit) 60-65%.

CoMo post frequency conversion detector

- **dbbcif(a|b|c|d)** = input_ch, attenuation, filter, target_agc_value, detector

detector => selection of one of the post conversion channel as detector for AGC.
If omitted the standard detector in the CoMo is used and '-1' indicated.

DDC v106 and v106E: novelties

- **cont_cal** = status, freq, option

Continuous calibration for noise diode activation.

status => on|off, freq, option

freq => rate of noise diode switching (in a range of about 8Hz - 300KHz)

option => 2 = output always ON, 5 = inverted polarity

- **'calib_vsi'** command for optimize the intra-stack data output propagation (in v106E only)

end of DBBC2
start of DBBC3

DBBC3 status and news

- **Hardware**

- **Firmware and Software**

New HARDWARE

- **GCAT**

  new synthesizer board, allows to adopt if required different reference frequencies (ex. 100MHz)

- **GPS_DISTRIBUTOR v2**

  a new GPS receiver compatible operating with GNSS, GALILEO, GLONASS, COMPASS, SBAS distributed to all the CORE3H boards

- **FILA RED v3**

  new interface for enabling PCI communication in addition to the serial one in the CORE3H

- **CPU board Advantech PCI7031 with SSD disk in VGOS systems**

FIRMWARE/SOFTWARE (1/2)

- **DUCS** (DBBC3 Unified Control Software)

✓ **Software to control all functions, including continuous calibration**
✓ **New advanced method to control the main samplers parameters, delay, gain and offset**
✓ **Commands and functions similar to the DBBC2 ones**

- **3DCS** (ready; direct conversion sampling)

✓ **Full 4/1 GHz band/IF direct conversion sampling**
✓ **Input in the range 0-4GHz / pre-filtered max 4 GHz bwd in the range 4-15 GHz**
✓ **Total power measurements in all the bands**
✓ **Standard output 4 SFP+ @ 4 Gbps for each CORE3H (each IF)**
✓ **EVN version with 2 IFs (4 GHz ea.), output 32 Gbps**
✓ **VGOS version with 8 IFs (4 GHz ea.), output 128 Gbps**

FIRMWARE/SOFTWARE (2/2)

- **3DDC** (in development)

✓ **Different modes possible: W1/W2/W3/B/E/F**

✓ **Different number of bbc depending on the selected mode**

✓ **128 MHz - 64 MHz - 32 MHz - 16 MHz - 8 MHz - 4 MHz - 2 MHz**

- **W1=> 128 MHz out, 4 GHz in**
- **W2=> 64 MHz out, 4 GHz in**
- **W3=> 32-16-8-4-2 MHz out, 4 GHz in**
- **F => 32-16-8-4-2 MHz out, 1 GHz in**
- **E => 32-16-8-4-2 MHz out, 512 MHz in**
- **B => 16-8-4-2-1 MHz out, 512 MHz in**

- **3PFB** (in development)

✓ **Different modes possible: W/B/F**

✓ **Different number of PFB blocks depending on the selected mode**

✓ **256 MHz - 64 MHz - 32 MHz**

- **W=> 256MHz out, 4 GHz in**
- **F => 64 MHz out, 1 GHz in**
- **B => 32 MHz out, 512 MHz in**