UniBoard^2
Measurement Report

	Organisatie / Organization	Datum / Date
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1 Introduction

In this report the measurement results for of the UniBoard2 proto type are presented. This document is used to verify the design principles of AD-1 and AD-2.

UniBoard^2 is a Joint Research Activity (JRA) in the RadioNet3 project, funded by the EC through the FP7 programme, under grant agreement no. 283393. The partners in this JRA are the Universities of Bordeaux and Orleans, INAF, MPG Bonn, the University of Manchester, ASTRON and JIVE.

1.1 Applicable documents (AD)

Ref.nr.	Document number	Title
AD-1	ASTRON-TN-042	UniBoard2 HW Detailed Design
AD-2	ASTRON-RP01484	UniBoard2 SI simulation

1.2 Reference documents (RD)

Ref.nr.	Document number	Title
RD-1	INFRA-2011-1.1.21 ASTRON-TN-040	Deliverable 8.2, Hardware Design Document
RD-2		
RD-3		

1.3 Abbreviations

AD-n	nth document in the list of Applicable Documents
BER	Bit Error Rate
BW	Band Width
DC	Direct Current
DCA	Digital Communication Analyzer
DC/DC	Converter from one DC voltage to another
DDR	Double Data Rate (memory protocol)
FPGA	Field Programmable Gate Array
JTAG	Joint Test Action Group (Protocol for Hardware testing)
PCB	Printed Circuit Board
POL	Point of load
PRBS	Pseudo Random Binary Sequence
RD-n	nth document in the list of Reference Documents
PMBus	Power Management Bus (I2C interface to SMPS)
TDR	Time Domain Reflectometry
SPD	Serial Presence Detect
SMPS	Switch mode Power Supply

1.4 Used Equipment

In Table 1 the equipment used during the measurements are shown.

Table 1 Used Equipment

Equipment	Type	Manufacturer	ZWO number
Power supply	N6705B	Agilent Technologies	ZWO2104
Oscilloscope	Infinium	HP	ZWO1797
DMM		Fluke	
JTAG controller	JT3707 + JT2148	JTAG Technologies	
Digital Communication Analyser (TDS+Scope)	DCA-J	Agilent	

2 Impedance

The impedance of the PCB is tests with the TDR. For this a test board is used. Only a few lines are measured, see Table 2.

Table 2 TDR results

Node	Type	Net	Layer	Measurement	Impedance [Ω]
0	Backplane Interface	RING_0_TX_x5	14	Node0_p1.bmp	100 -0.2 +17
0	Backplane Interface	RING_0_TX_x4	16	Node0_p2.bmp	100 -0.1 +14
0	Backplane Interface	RING_0_RX_x5	7	Node0_p3.bmp	100 -0.1 +13
0	Backplane Interface	RING_0_RX_x4	5	Node0_p4.bmp	100 -0.1 +4
3	Backplane Interface	RING_1_RX_x5	7	Pair1b.bmp	100 -0.1 +10
3	Backplane Interface	RING_1_RX_x2	5	Pair2b.bmp	100 -0.1 +7
3	Backplane Interface	RING_1_TX_x1	14	Pair3b.bmp	100 -0.1 +4
3	Backplane Interface	RING_1_TX_x0	16	Pair4b.bmp	100 -0.1 +4
0	QSFP Interface	QSFP_1_TX_x3	3	Qsfp_node0.bmp	100 -0.2 +4
3	QSFP Interface	QSFP_5_TX_x3	5	Qsfp_node3.bmp	100 -0.5 +2

In Figure 1 the TDR measurement result for RING_0_TX_x5 is shown. At the start a large change in impedance is seen, this is due to the coupling of the test fixture. The line is not terminated, this means that the reflection is high. Close to the end of the line a large bump is seen. From this measurement it can be seen that in impedance in close to 100Ohm, expect a small bump at the end. From the trace layout in Figure 2 it can be seen that this might be caused by the rounding of the mounting hole.

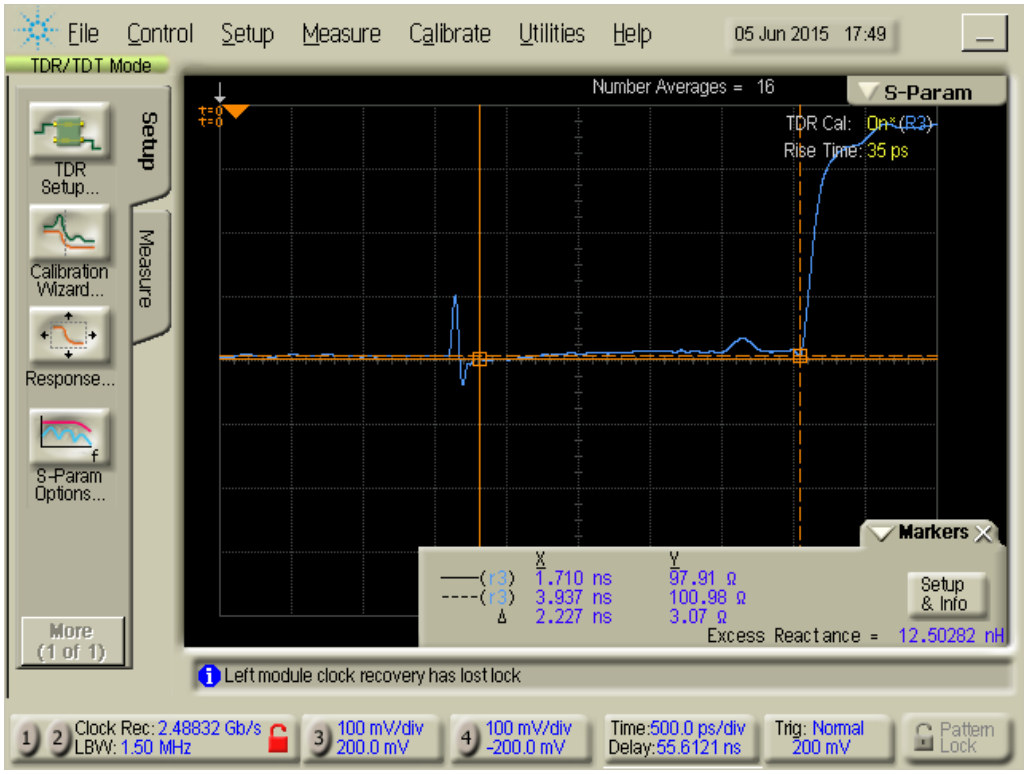

Figure 1 TDR measurement result for RING_0_TX_x5

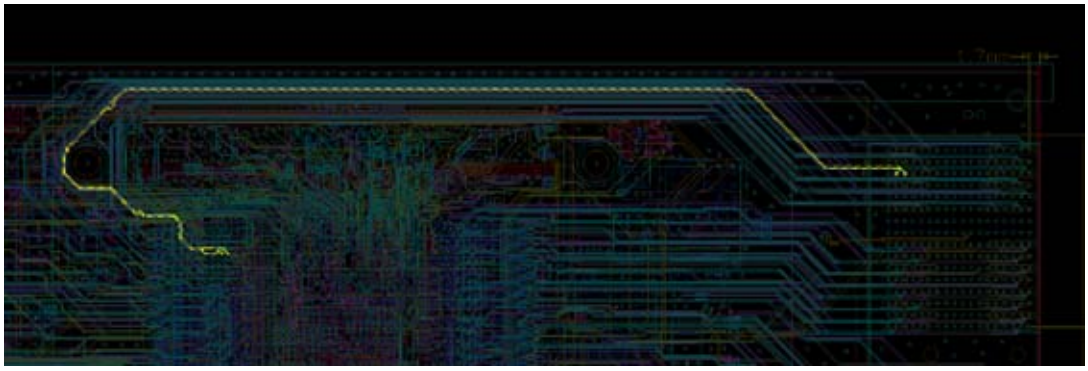

Figure 2 Layout of RING_0_TX_5x

Given the length of the line, 812.78mm, the time for a single direction of 1.11ns, the ε_r can be estimates at 3.3, close to the design parameter of 3.6. ((300e6*1.11e-9)/182e-3)^2

3 Power up

Before power-up the impedances of the board are measured, see Table 3. Because all impedances are >10Ω the power of the board is switch on and the supply voltages are measured with the digital multimeter. The Ericsson SMPS are incorporated with readout possibilities and a PMBus. The readout values are shown in Table 3.

Table 3 Central Power supplies (unconfigured FPGAs)

Supply	Impedance	Voltage	Expected voltage	I2C Address	Current	Max exp	Mes. Power
48V Input UniBoard2	10kΩ	48V	48V		1.25A		60W
Output PIM	600kΩ	47.7V	48V				
Hold-up PIM	1.4MΩ	75V	75V				
Output Bus converter	190kΩ	12V	12V	0x2C	4.5A		54W
VCC_QSFP_N01	320kΩ	3.30V	3.3V	0x02h	2.3A	13A	7.6W
VCC_QSFP_N23	200kΩ	3.30V	3.3V	0x01h	0.7A	13A	2.3W
VDD_CLK	113Ω	2.50V	2.5V	0x0Dh	1.1A	2A	2.8W
Switch IO (3V3)	500Ω	3.29V	3.3V	0x0Eh	0.4A	2A	1.32W
Switch Core (1V2)	290Ω	1.20	1.2V	0x0Fh	1	3A	1.2W

From the power result it can be seen that 6W is used in the PIM, 2.5W in the switch, 10W in the QSFP logic and 2.8W for the clock, resulting in approx 22W board overhead and 9.5W per FPGA.

Table 4 Node supplies with FPGAs in reset

Supply	Impedance	Voltage	Expected voltage	I2C Address	Current	Max exp	Mes. Power
1V8	380Ω	1.79V	1.8V	0x11h	0.3A	2A	0.5W
VCC (core)	2Ω	0.96V	0.95V	0x01h	4.7A	30A	4.5W
VCCERAM	110Ω	0.95V	0.95V	0x0Dh	0.2A	10A	0.2W
VCCR_GXB	37Ω	1.00V	1.0V	0x0Eh	0.5A	10A	0.5W
VCCT_GXB	63Ω	1.00V	1.0V	0x0Fh	0.3A	5A	
VCC_BAT 1V8	14Ω	1.80V	1.8V	0x10h	0.7A	6A	
VCCH_GXB	14Ω	1.80V	1.8V	Via 0x10h		3A	
VCCPT	15Ω	1.79V	1.8V	Via 0x10h		1A	
VCC_Fuse	3.2kΩ	2.20V	2.2V	-			
VCC DDR	96Ω	1.20V	1.2V	-			
VTT DDR	300kΩ	0.60V	0.6V	-			
VREF DDR	250kΩ	0.60V	0.6V	-			

From the power result it can be seen that 6W is used by the measured power supply, this means that 3.5W is used for the DDR4 power supplies and the POL overhead.

3.1 Power Sequencing

As described in AD-1 the different powers of the FPGA should be switch on at a given sequence. In Figure 3 the sequence is repeated.

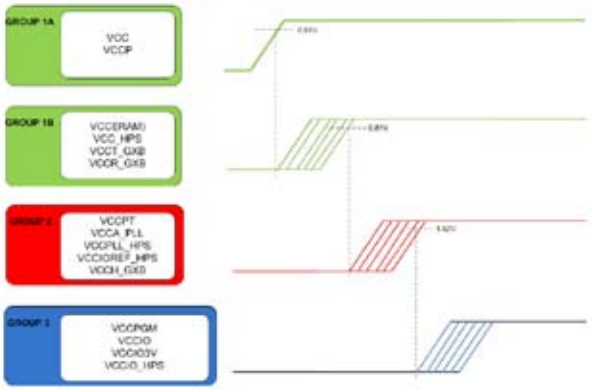

Figure 3 Power Sequence Reference diagram

The measurement is done to verify the on-sequence, see Figure 4 and Figure 5.

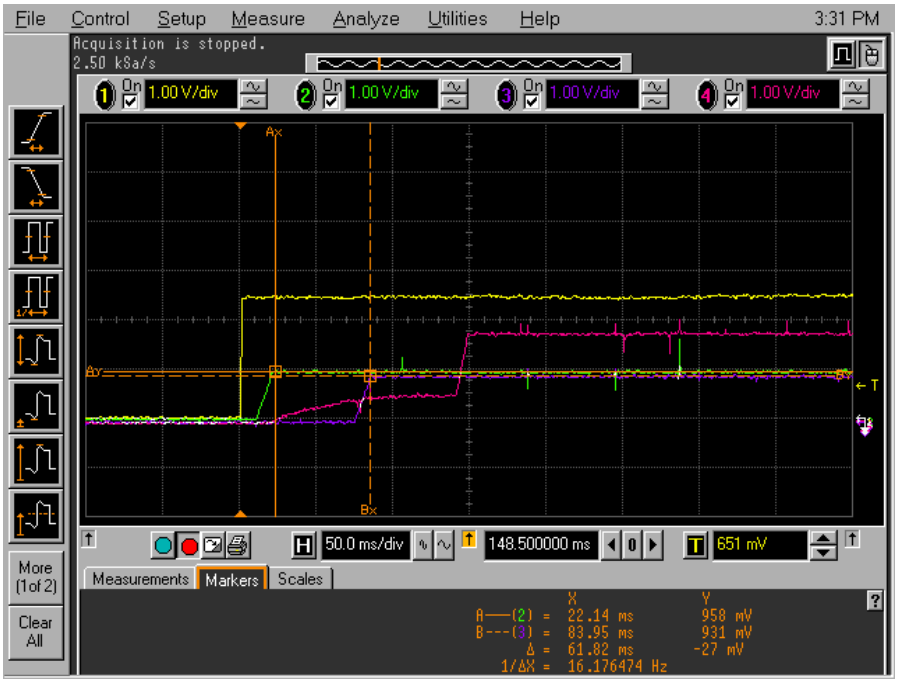

Figure 4 Sequence ON showing on/off (yellow), Vcc_core (green), Vcc_eram (purple) and Vcc_bat (pink)

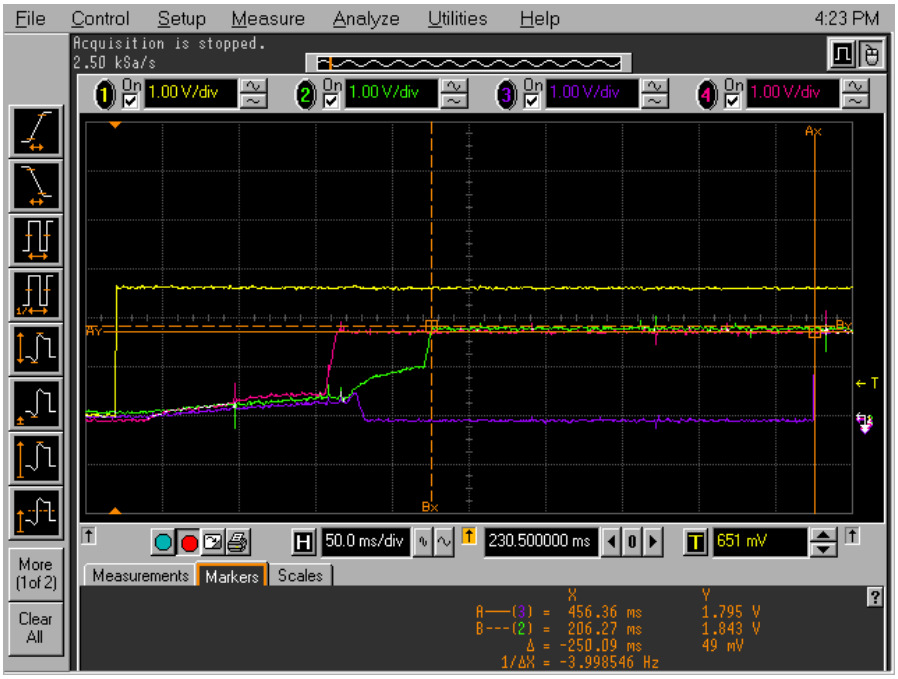

Figure 5 Sequence ON showing on/off (yellow), Vcc_bat (pink), Vcc_io (green) and Config (purple)

From this measurement it can be seen that all supplies switch on according the specifications. The release of the CONFIG signal, indicating configuration of the FPGA, is added. The CONFIG line is released 250ms after the last power is available.

The measurement result of the off-sequence measurement is shown in Figure 6 and Figure 7.

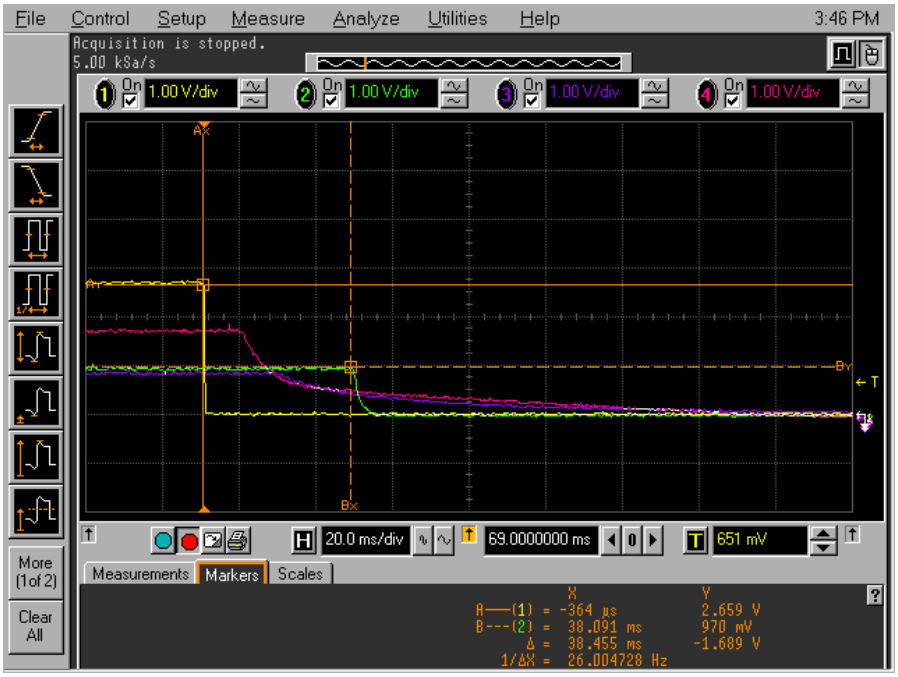

Figure 6 Sequence OFF showing on/off (yellow), Vcc_core (green), Vcc_eram (purple) and Vcc_Bat (pink)

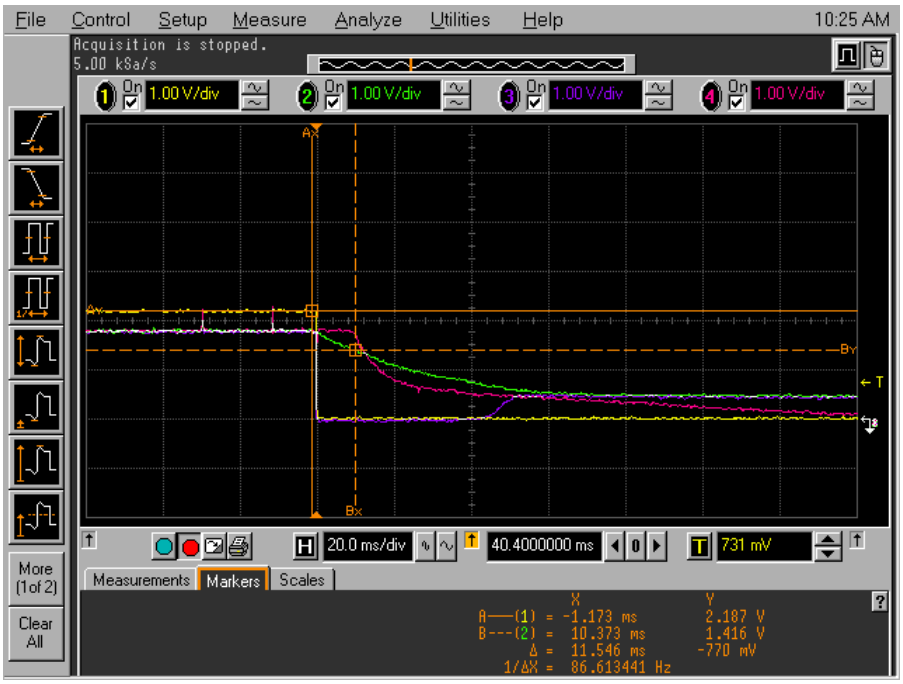

Figure 7 Sequence OFF showing on/off (yellow), Vcc_bat (pink), Vcc_IO (green) and CONFIG (purple)

From this measurement it can be seen that the FPGAs are placed in reset direct at a falling edge of the ON/OFF, thereby reducing the power consumption. The IO voltage is switched off first. The capacitance of the IO voltage is however on the large side, this result in holding up the power longer than wanted.

To see the effect of switching off the power to UniBoard, first a measurement is done by button switch off, see Figure 8, where a marker is placed at the switch off of the last power supply the VCC_{core}.

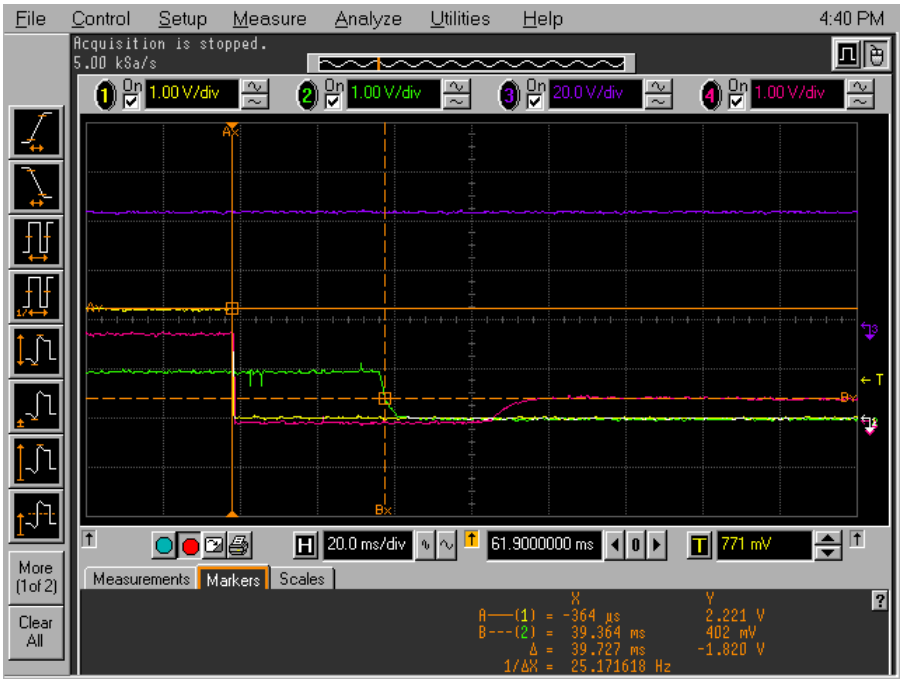

Figure 8 Board off with button showing on/off (yellow), Vcc_core (green), Vcc_IO (pink), VDD_input (purple)

After this measurement, the measurement is repeated by switching off the power to the board. The result is shown in Figure 9.

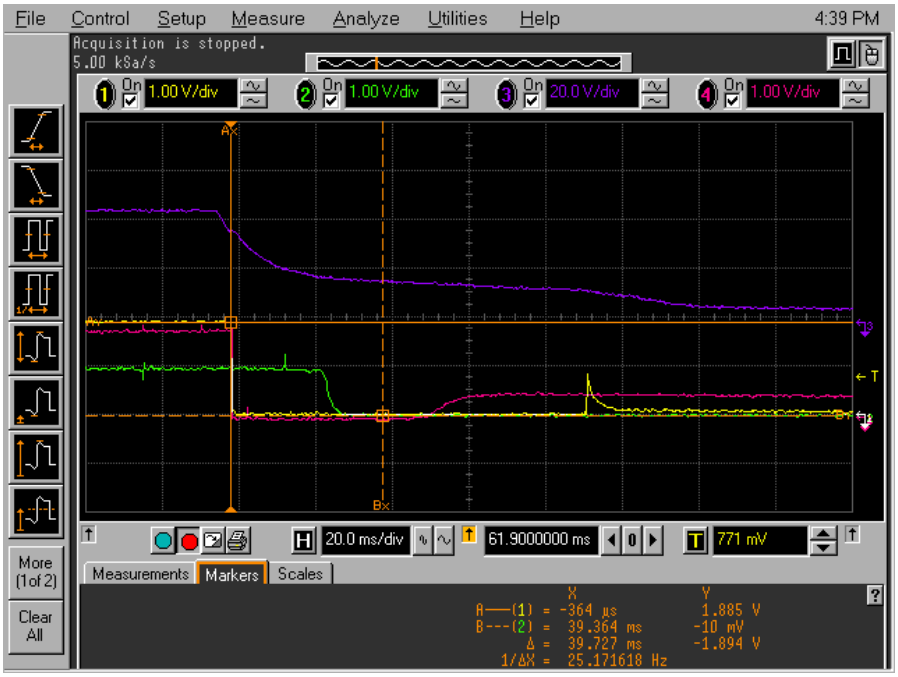

Figure 9 Board off with power off, showing on/off (yellow), Vcc_core (green), Vcc_IO (pink), VDD_input (purple)

From this measurement it can be seen that the core supply is switch off before the expected time. In Figure 10 the power at the input of the VCC_{core} POL is shown, together with the input power of the Bus converter (converting 48V to 12V).

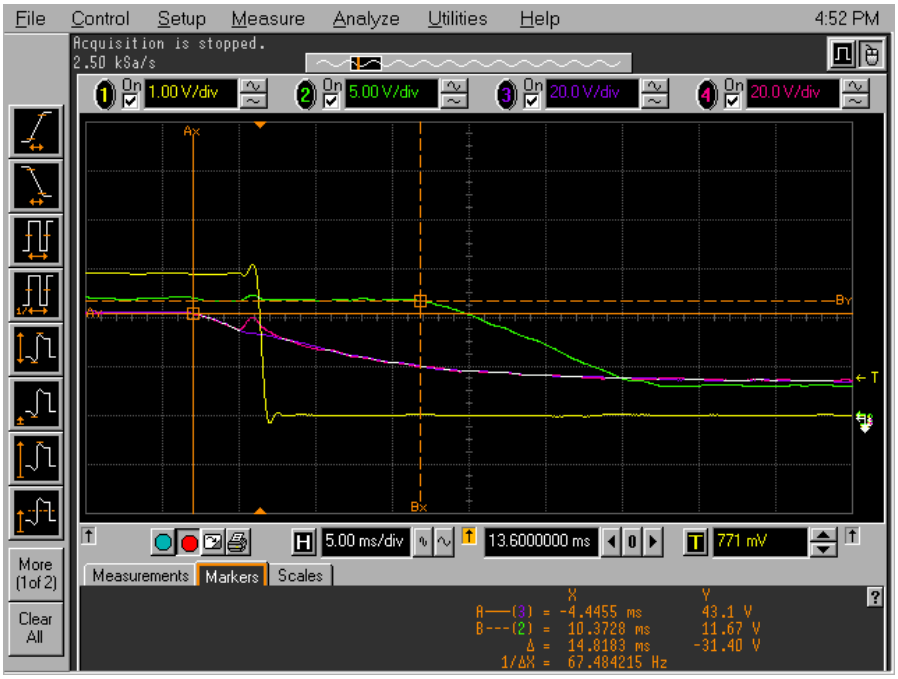

Figure 10 Switch off, showing on/off (yellow), Vcc_12V (green), Vcc_UNB2in (purple), Vcc_brick_in (pink)

From this measurement it can be seen that input voltage of the bus converter is not extended beyond the input of the PIM. The hold-up function of the PIM should take care of this.

For the calculation of the hold-up time the power to hold up is estimated 60W, the time for hold-up is estimated 40ms. This results with the current capacitor of 330uF is:

$C_{holdup} = (2*P*t) /(Vhu^2 – Vth^2)$ →

$t = C*(Vup^2 – Vth^2)/(2*P) = 330uF(75^2-36^2)/(2*60) = 11ms$

3.2 1000uF Hold-up

The 330uF Hold up capacitor is replaced by a 1000uF capacitor for testing. With all FPGAs configured, UniBoard^2 running at 200W, the power supply is switched off. The result of the measurement is shown in 12V and the VCC_{core} are shown in Figure 11, in this figure the green line is ON/OFF, the pink line VCC_{core}, the purple line 12V. The dashed marker indicates the falling edge of the VCC_{core} during normal on-off by the button. From this measurement it can be seen that the hold on is at the limit (12V is going down before the core is switched off, but the there is enough capacitance in the 12V bus supply to keep the level at the input of the SMPS enough to enable 12V conversion to 0.9V for VCC_{core}.

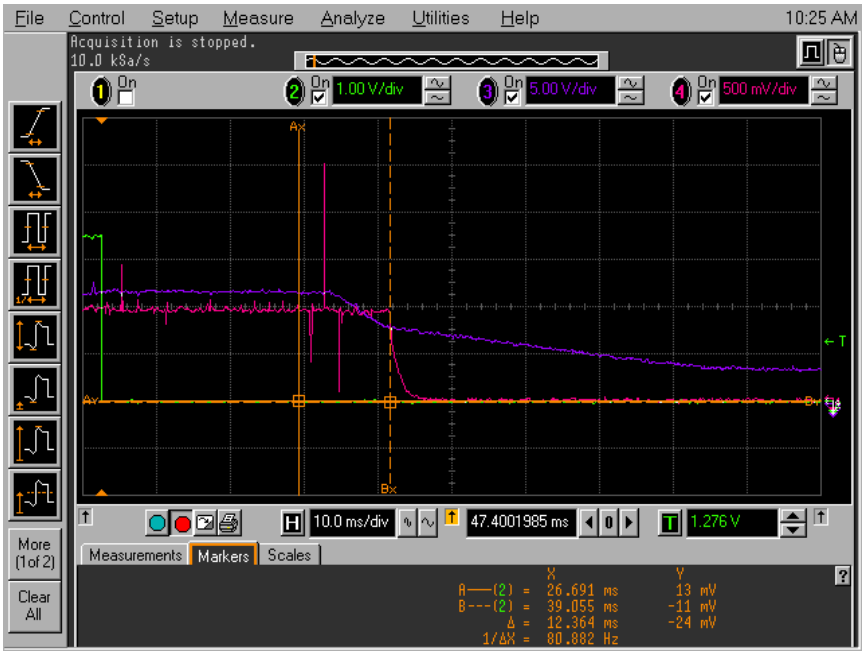

Figure 11 Hold up with 1000uF capacitor.

This measurement shows that a 1000uF capacitor is the best value to have a controller down sequence.

3.3 Input Current

The input current of the board is measured by the power N6705B DC Power Analyser, see Figure 12.

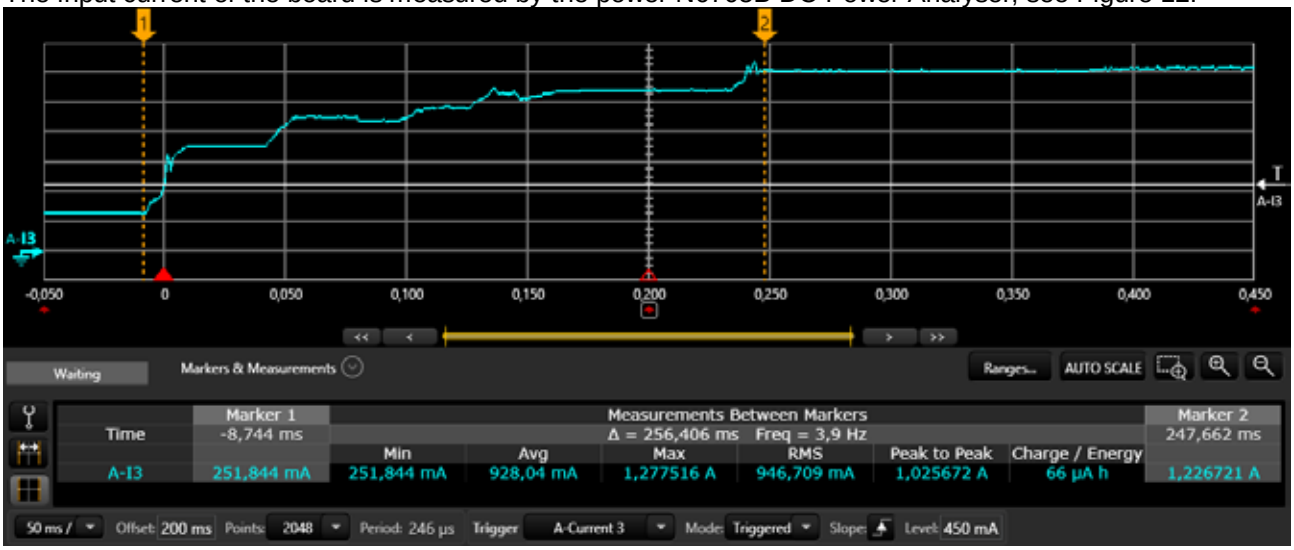

Figure 12 UniBoard^2 input current at Switch ON

From this measurement the sequencing of the power supplies is clearly seen. The measurement is repeated at switch off, see Figure 13

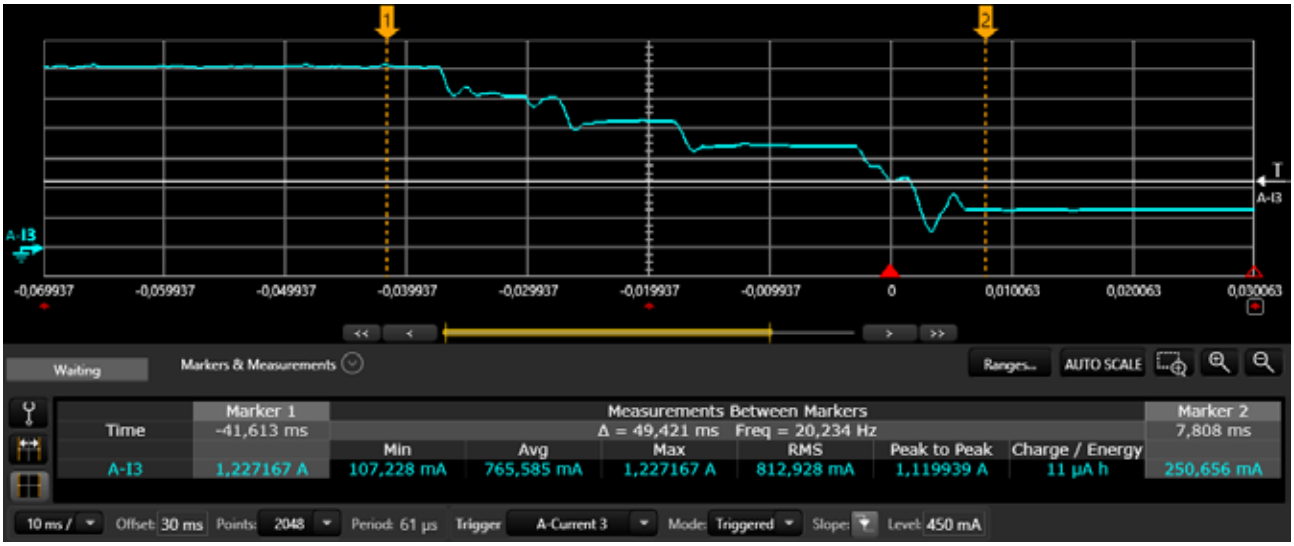

Figure 13 Switch off

With a marker placed at switch off and one at the end point the energy is measured during shut down. The capacitance needed to switch down can be estimated with the definition of a capacitor: 1F =1A/s/V.

(11*10^-6)*3600/75V = 528uF

4 Boundary Scan

4.1 Standard Tests

For the boundary scan JTAG Technologies Provision version CD21 has been used. For the test of the interconnections between the FPGA and the DDR4 sockets test board have been made where 100Ω resistors are placed between two lines, see Figure 14.

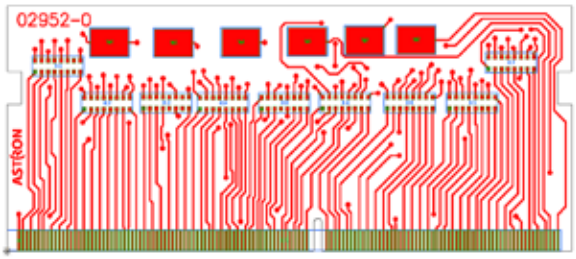

Figure 14 DDR4 Test board

For boundary scan the following tests are made.

Table 5 JTAG tests

Test	Testing
Interconnection	Infrastructure, and general interconnection tests.
Inter_ddr	General interconnection + all DDR4 connectors
Transc_QSFP_node0	Transceiver test for Ring transceivers between FPGAs and all QSFP cages for Node 0
Transc_QSFP_node1	Transceiver test for Ring transceivers between FPGAs and all QSFP cages for Node 0
Transc_QSFP_node2	Transceiver test for Ring transceivers between FPGAs and all QSFP cages for Node 0
Transc_QSFP_node3	Transceiver test for Ring transceivers between FPGAs and all QSFP cages for Node 0

The testability can be calculated, the result is shown below.

```
Net Statistics                                  Testability    % Coverage    %
================================================================================
Total number of nets calculated                        4893 100%     4893 100%
      Nets in Netlist                                  4792           4792
      Nets added for not connected pins (+)             101            101
      Nets ignored by user (-)                            0              0

Sensed and driven nets                                 2041  42%     1471  30%
      Sensed by BSCAN device (direct)                  1654           1179
      Sensed through transp. device (indirect)          230            145
      Sensed Pwr / Gnd nets                              45             45
      Implicitly tested nets                            112            102

      Nets Covered 100% by user                                          0
      Nets Covered by JFT                                                0
      Nets Covered by Imported CSV File                                  0

Nets not tested by BSCAN                               2852  58%     3422  70%


--             Device statistics report            --

Device Statistics                               Testability    % Coverage    %
================================================================================
Total number of devices calculated                     5649 100%     5649 100%
      Devices in Netlist                               5649           5649
      Devices excluded by Bill of Materials (-)           0              0
      Ignored Devices (-)                                 0              0

Devices involved in a BScan test                        535   9%     2881  51%
      BSCAN devices                                       6              6
      Devices under test (50% - 100%)                   529           2874
      Devices under test (0% - 49%)                       0              1

      Devices Covered 100% by user                                       0
      Devices Covered by JFT                                             0
      Devices Covered by Imported CSV File                               0

Devices without BSCAN testability                      5114  91%     2768  49%
      Devices without model                            1100           1100
      Devices not testable according to user              0              0
      Capacitors                                       3319            699
      Other devices                                     695            969
```

4.2 JTAG Functional Test (JFT)

With Provision's JFT all IO pins can be accessed by Python scripts. This has been used to test all I2C interfaces on UniBoard^2. In Table 6 the tests are described.

Table 6 JFT tests

Test	Testing
JFT_EEPROM	Testing the EEPROM by writing and reading data
JFT_LOC_PWR	Testing the interface to the local power supplies. This is done by reading out the current and the voltage of one POL
JFT_BRD_PWR	Test to verify the Node2 connection to the central power and the temperature sensor of the Ethernet Switch.
JFT_SPD_DDR	Verify the I2C interface to the SPD of the DDR4 module. This is down for the temperature sensor and by reading out the part number
JFT_QSFP_READ	Verify the six individual I2C interface to the six modules per FPGA. This is done by reading out the temperature and the voltage on the module.

In Figure 15 and example of an I2C sequence is shown. In this measurement it can be seen that the minimal clock is 63Hz. For some parts (like the BMR464 used for VCC_{core}) this clock is to slow, these SMPSs have to be tested with functional hardware.

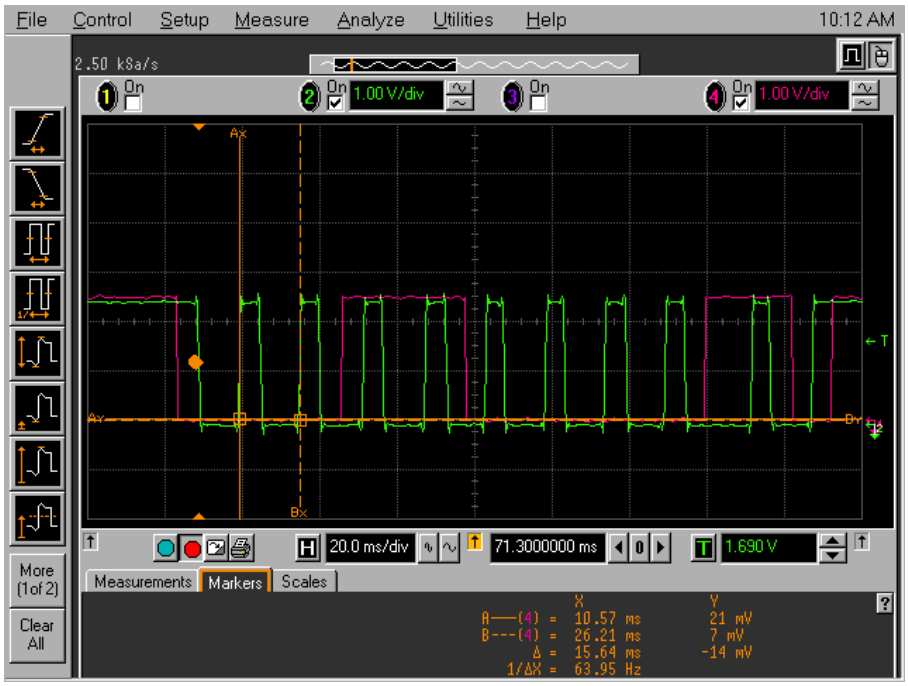

Figure 15 JFT I^2C sequence

As an example the test result for the SPD DDR is shown in Figure 16.

Node	Slot	TEMP	Part Number
0	0	35.75	18ASF1G72HZ-2G1A1 '
0	1	36.25	18ASF1G72HZ-2G1A1
1	0	36.50	18ASF1G72HZ-2G1A1
1	1	37.00	18ASF1G72HZ-2G1A1
2	0	31.25	18ASF1G72HZ-2G1A1
2	1	35.25	18ASF1G72HZ-2G1A1
3	0	27.00	18ASF1G72HZ-2G1A1
3	1	29.50	18ASF1G72HZ-2G1A1

Figure 16 JFT test for the DDR SDP.

5 Ethernet communication

The Ethernet communication is tested with the test firmware loaded in the FPGA. The result is shown Figure 17.

```
[2015:06:05 16:38:05] - (0) UTIL - >>> Title : Utility for pi_system_info.py on
UNB-[63], FN-[0, 1, 2, 3]
[2015:06:05 16:38:05] - (3) UTIL - SI - UNB-63, FN-0:     Design = unb2_test_1GbE
[2015:06:05 16:38:05] - (3) UTIL - SI - UNB-63, FN-1:     Design = unb2_test_1GbE
[2015:06:05 16:38:05] - (3) UTIL - SI - UNB-63, FN-2:     Design = unb2_test_1GbE
[2015:06:05 16:38:05] - (3) UTIL - SI - UNB-63, FN-3:     Design = unb2_test_1GbE
```

Figure 17 Results of first communication

The status of the switch is readout by the RS232 control interface. For this Realterm is used where the interface is set to 8 data bits, 1 stop bit, no parity 9600 baud. The result is shown in Figure 18 and Figure 19.

```
UniBoard2 0.4
UniBoard2
Length Jumbo:  9600
Chip id: 273890e9

PRT0 PRT1 PRT2 PRT3 PRT4 PRT5 PRT6 PRT7 PRT8 PRT9 PRT10 PRT11 PRT12 PRT13
N0-0 N0-1 N1-0 N1-1 N2-0 N2-1 N3-0 N3-1 C ll C ul C lm  C um  C lr  C ur
```

Figure 18 Result of 'V' command on the switch

```
Port Status     RXOCT        TXOCT
 0   Port Up    0x00000000   0x00000000
 1   Port Down  0x00000000   0x00000000
 2   Port Up    0x00000000   0x00000000
 3   Port Down  0x00000000   0x00000000
 4   Port Up    0x00000000   0x00000000
 5   Port Down  0x00000000   0x00000000
 6   Port Up    0x00000000   0x00000000
 7   Port Down  0x00000000   0x00000000
 8   Port Down  0x00000000   0x00000000
 9   Port Up    0x00000000   0x00000000
10   Port Down  0x00000000   0x00000000
11   Port Down  0x00000000   0x00000000
12   Port Down  0x00000000   0x00000000
13   Port Down  0x00000000   0x00000000
```

Figure 19 Result of 'S' command on the switch.

6 CONFIG

After some modification Quartus II programmer is used to program the flash.

7 DDR4 test

The DDR4 are tested with the use of the EMIF toolkit. An example of the calibration report is shown in chapter 10.
After all parameters are set for the calibration the design is included in UNB2_test. A python test case is used to test both memory banks for large package sizes.

```
[2015:08:13 15:48:26] - (3) TB - >>>
[2015:08:13 15:48:26] - (1) TB - >>> Title : Test case for the unb2_test_ddr design with MB = I on
UNB-[0], GN-[0, 1, 2, 3]:
[2015:08:13 15:48:26] - (3) TB - >>>
[2015:08:13 15:48:26] - (3) TB -
[2015:08:13 15:48:26] - (3) TB - >>> Rep-0
[2015:08:13 15:48:33] - (3) TB - UNB-0, FN-0: RX_SEQ read_result = Data OK
[2015:08:13 15:48:33] - (3) TB - UNB-0, FN-1: RX_SEQ read_result = Data OK
[2015:08:13 15:48:33] - (3) TB - UNB-0, FN-2: RX_SEQ read_result = Data OK
[2015:08:13 15:48:33] - (3) TB - UNB-0, FN-3: RX_SEQ read_result = Data OK
[2015:08:13 15:48:33] - (3) TB -
[2015:08:13 15:48:33] - (3) TB - >>>
[2015:08:13 15:48:33] - (0) TB - >>> Test bench result: PASSED
[2015:08:13 15:48:33] - (0) TB - >>> Runtime=6.220504 seconds (0.001728 hours)
[2015:08:13 15:48:33] - (3) TB - >>>
```

Figure 20 DDR test results

The reference clock for the DDR is shown in Figure 21.

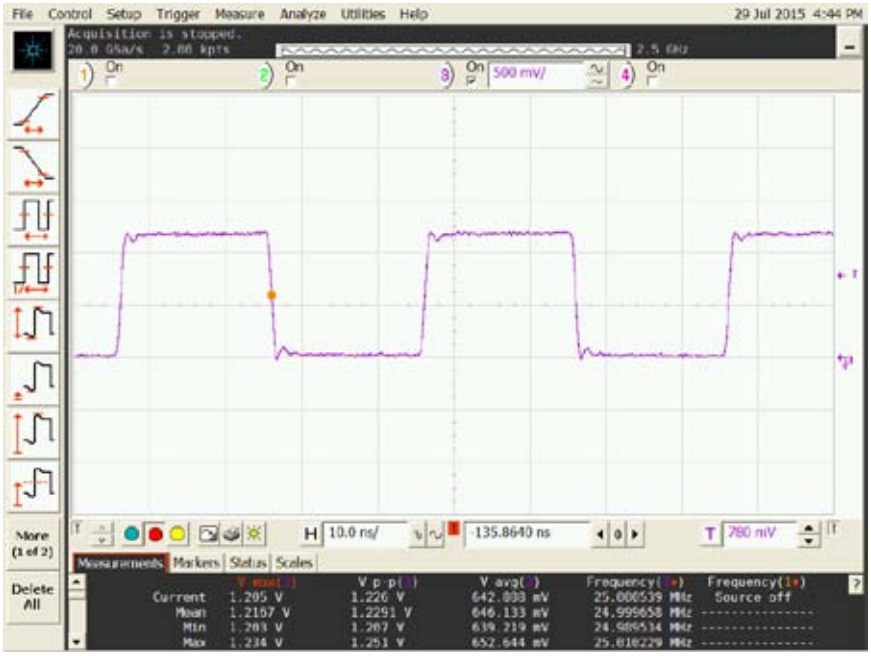

Figure 21 DDR reference clock

8 SerDes

The transceivers are tested with the Transceiver Toolkit as part of Quartus II version 15.0.1. The power consumption for different number of used transceivers is shown in Table 7. For the measurement of 96 transceivers the VCCR-GXB and VCCT_GXB are connected together underneath the FPGA.

Table 7 Power consumption as function of the number of transceivers.

Power	MAX Current	Boot image	24 Trans.	48 Trans.	72 Trans.	96 Trans.
VCCR_GXB	12A	0.6A	4.0A	7.3A	11.6A	10.6A
VCCT_GXB	12A	0.3A	1.2A	1.9A	3.2A	9.3A
VCC_CORE	40A	2.1A	4.6A	7.3A	9.7A	14.7A
VCC_BAT	12A	1.0A	2.8A	4.3A	6.4A	8.5A
VCC_ERAM	12A	0.2A	0.2A	0.2A	0.2A	0.3A
VCC_IO	12A	0.1A	0.1A	0.1A	0.1A	0.1A

From this table it can be seen that the power consumption per transceiver is in the order of 0.2W (0.15W for Rx and 0.05W for Tx).
For the transceiver test the build in PRBS 31 is used. On the receiver a checker is used to calculate the BER. In Figure 22 the interfaces of the ring are shown. The output is sorted on Bit errors.

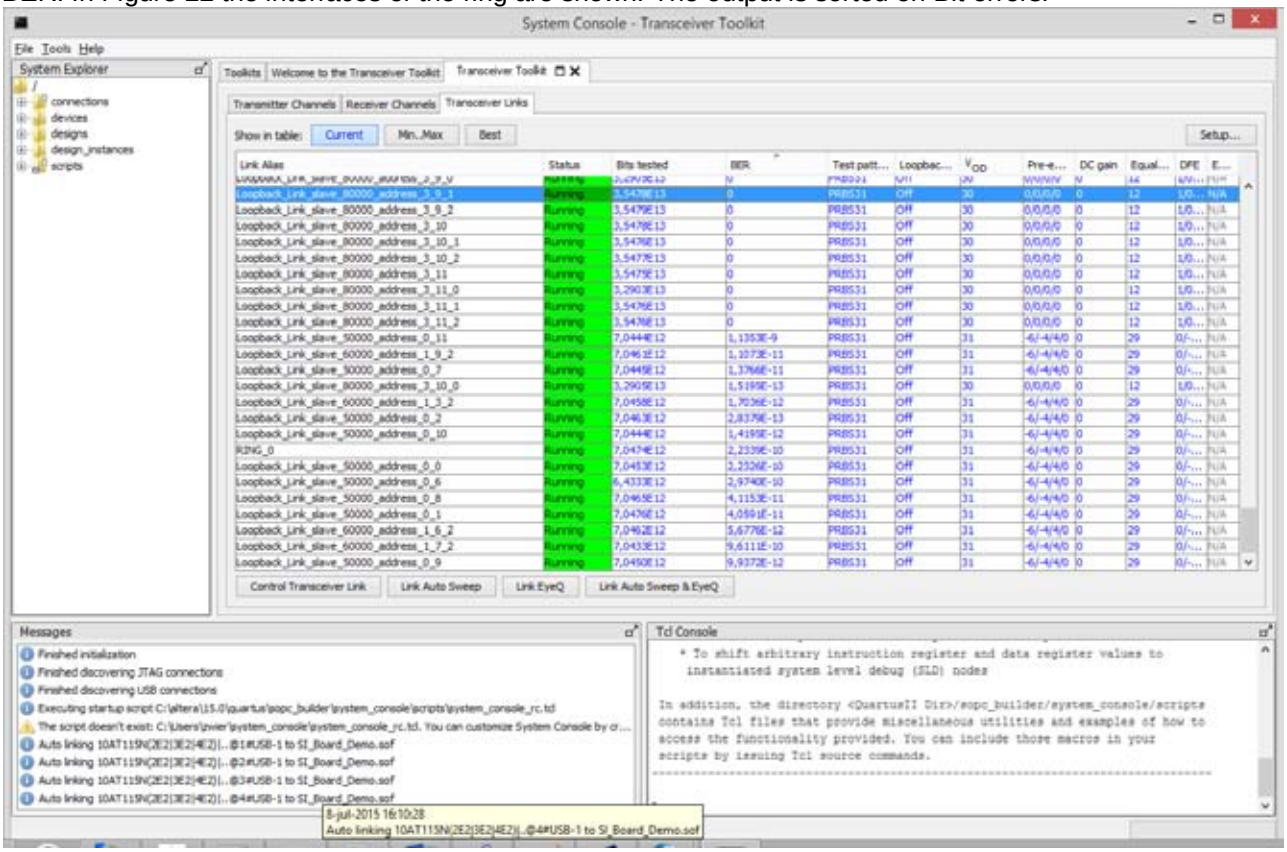

Figure 22 Screen Dump Transceiver Toolkit with Ring interfaces

In this table the net names are:

Loopback_link_slave_?000_address_<bus>_<lane>_<node-1>
Bus 0, ring 0
Bus 1, ring 1
Bus 2 and 3 backplane

From this result it can be seen that some links have a high BER >1e-12. These links are from Node 0 ring 0 (Loopback_link_slave_5000_address_0_<lane>) to/from Node 3 ring 1 (Loopback_link_slave_6000_address_1_<lane>_2). The link between node 0 and node 3 on UNB2_TB has long traces. Because the test board uses standard FR4, it shows that not all PCB loss can be compensated. On the ES1 devices the 10GbE option for Backplanes is not available. Better results are expected with this option. Another option to compensate for PCB losses is the use of a better PCB material like Megtron6. On the production boards with production Arria10 device will be placed better PLLs and some extra options for

compensating loss can be used. It is expected with the right material and the production devices it should be possible to make a links of 300 mm

In Figure 23 the results for the QSFP and the backplane interfaces are shown. On the QSFP a combination of copper and optical interfaces are used. All interfaces are within the expected 1e-12.

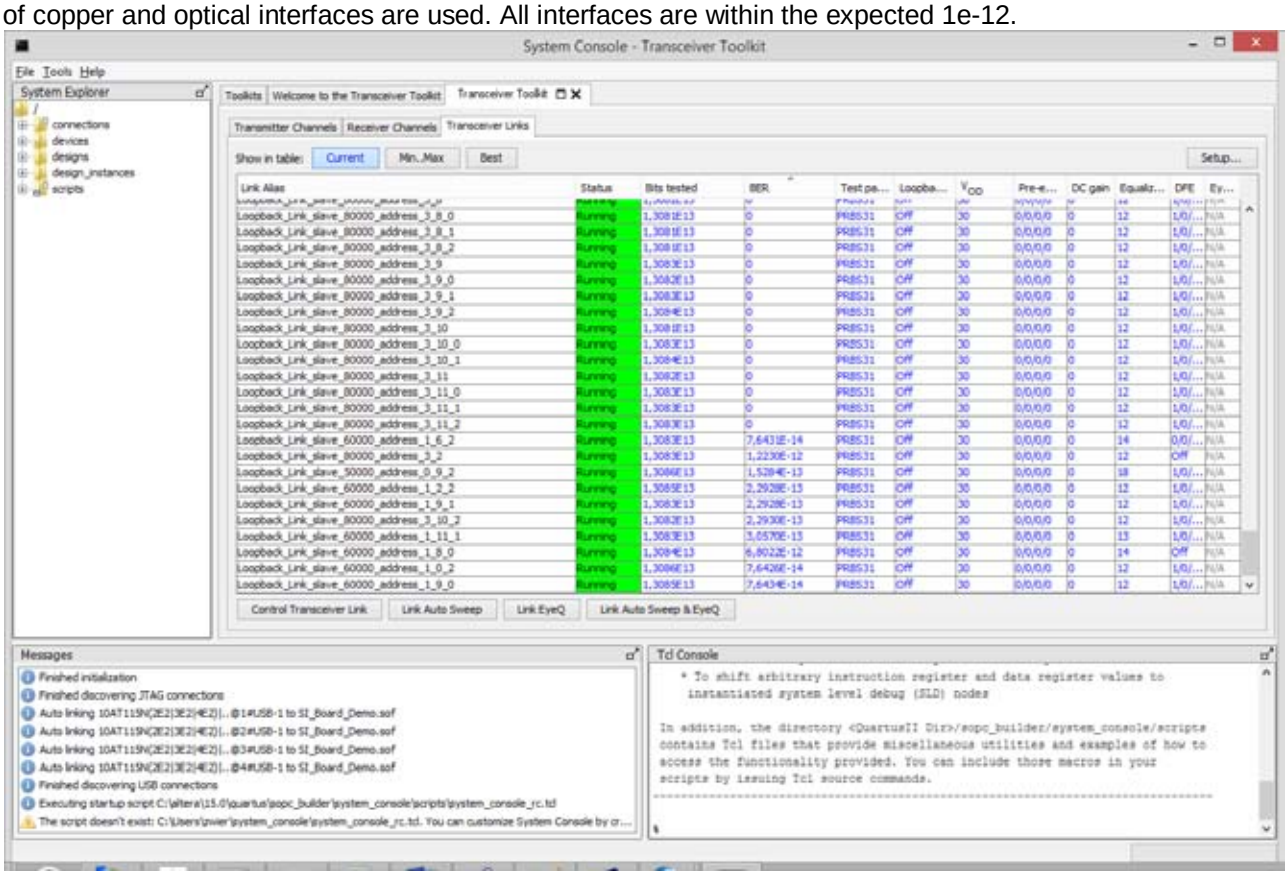

Figure 23 Screen dump QSFP + Backplane

In this table the names of the transceivers are:
Loopback_link_slave_?000_address_<bus>_<lane>_<node-1>
Bus 0 and 1 QSFP cages 0-6
Bus 2 and 3 backplane

9 Conclusion

After some modification UniBoard^2 is working. The ES device maximum speed of 1600MT/s of the Memories are reached. Some errors in transceiver lines are seen. It is expected with that with the production devices speeds of 10Gbps can be achieved. !

10 Memory Calibration Report

```
Calibration Report report for ed_synth
Thu Aug 13 10:56:48 2015
Quartus II 64-Bit Version 15.0.2 Build 153 07/15/2015 SJ Full Version


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  7. Address/Command Margins Observed During Calibration
  8. VREF Margins Observed During Calibration



----------------
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authorized distributors.  Please refer to the applicable
agreement for further details.



+------------------------------+
; Calibration Status Per Group ;
+-------+--------+-------------+
; Group ; Status ; Error Stage ;
+-------+--------+-------------+
; 0     ; Pass   ; N/A         ;
; 1     ; Pass   ; N/A         ;
; 2     ; Pass   ; N/A         ;
; 3     ; Pass   ; N/A         ;
; 4     ; Pass   ; N/A         ;
; 5     ; Pass   ; N/A         ;
; 6     ; Pass   ; N/A         ;
; 7     ; Pass   ; N/A         ;
; 8     ; Pass   ; N/A         ;
+-------+--------+-------------+


+-------------------------------------------------------------------------------+
; DQ Pin Margins Observed During Calibration                                     ;
+--------+------------------+----------------+-------------------+-----------------+
; DQ Pin ; Read Margin (ps) ; DQ Input Delay ; Write Margin (ps) ; DQ Output Delay ;
+--------+------------------+----------------+-------------------+-----------------+
; 0      ; -180 to 180      ; 6              ; -180 to 180       ; 566             ;
; 1      ; -180 to 184      ; 3              ; -162 to 171       ; 564             ;
; 2      ; -192 to 192      ; 5              ; -180 to 180       ; 565             ;
; 3      ; -192 to 196      ; 0              ; -171 to 171       ; 563             ;
```

```
; 4      ; -168 to 172      ; 6              ; -189 to 189       ; 567             ;
; 5      ; -180 to 180      ; 2              ; -171 to 171       ; 563             ;
; 6      ; -184 to 188      ; 4              ; -198 to 207       ; 569             ;
; 7      ; -188 to 188      ; 3              ; -153 to 162       ; 562             ;
; 8      ; -180 to 180      ; 12             ; -162 to 171       ; 603             ;
; 9      ; -196 to 196      ; 6              ; -162 to 171       ; 594             ;
; 10     ; -180 to 184      ; 7              ; -144 to 153       ; 595             ;
; 11     ; -184 to 184      ; 6              ; -162 to 171       ; 597             ;
; 12     ; -188 to 192      ; 10             ; -162 to 171       ; 598             ;
; 13     ; -204 to 204      ; 0              ; -162 to 162       ; 595             ;
; 14     ; -180 to 184      ; 4              ; -162 to 171       ; 596             ;
; 15     ; -192 to 192      ; 14             ; -162 to 162       ; 600             ;
; 16     ; -168 to 168      ; 14             ; -162 to 162       ; 552             ;
; 17     ; -184 to 184      ; 3              ; -162 to 162       ; 548             ;
; 18     ; -180 to 184      ; 9              ; -162 to 171       ; 551             ;
; 19     ; -184 to 188      ; 8              ; -162 to 171       ; 549             ;
; 20     ; -176 to 180      ; 7              ; -162 to 171       ; 549             ;
; 21     ; -188 to 192      ; 0              ; -171 to 180       ; 550             ;
; 22     ; -172 to 176      ; 9              ; -171 to 171       ; 554             ;
; 23     ; -184 to 188      ; 8              ; -180 to 189       ; 552             ;
; 24     ; -172 to 172      ; 13             ; -171 to 180       ; 622             ;
; 25     ; -184 to 184      ; 0              ; -162 to 162       ; 613             ;
; 26     ; -176 to 176      ; 9              ; -189 to 189       ; 619             ;
; 27     ; -168 to 172      ; 20             ; -171 to 171       ; 624             ;
; 28     ; -184 to 184      ; 19             ; -171 to 171       ; 621             ;
; 29     ; -180 to 184      ; 7              ; -180 to 180       ; 618             ;
; 30     ; -180 to 180      ; 15             ; -180 to 180       ; 621             ;
; 31     ; -176 to 176      ; 23             ; -180 to 180       ; 624             ;
; 32     ; -168 to 172      ; 6              ; -189 to 189       ; 653             ;
; 33     ; -176 to 180      ; 1              ; -189 to 189       ; 650             ;
; 34     ; -156 to 160      ; 0              ; -180 to 180       ; 652             ;
; 35     ; -176 to 176      ; 9              ; -180 to 180       ; 655             ;
; 36     ; -168 to 168      ; 5              ; -171 to 171       ; 654             ;
; 37     ; -164 to 168      ; 3              ; -171 to 171       ; 651             ;
; 38     ; -172 to 172      ; 1              ; -189 to 198       ; 654             ;
; 39     ; -184 to 188      ; 8              ; -180 to 189       ; 655             ;
; 40     ; -172 to 172      ; 2              ; -180 to 189       ; 719             ;
; 41     ; -172 to 172      ; 7              ; -180 to 180       ; 719             ;
; 42     ; -168 to 172      ; 0              ; -171 to 171       ; 718             ;
; 43     ; -184 to 184      ; 8              ; -180 to 189       ; 719             ;
; 44     ; -172 to 176      ; 4              ; -171 to 180       ; 719             ;
; 45     ; -192 to 192      ; 16             ; -189 to 198       ; 722             ;
; 46     ; -180 to 180      ; 2              ; -171 to 180       ; 716             ;
; 47     ; -180 to 184      ; 12             ; -162 to 162       ; 721             ;
; 48     ; -176 to 180      ; 3              ; -171 to 171       ; 667             ;
; 49     ; -176 to 180      ; 4              ; -180 to 180       ; 670             ;
; 50     ; -156 to 160      ; 11             ; -171 to 171       ; 671             ;
; 51     ; -176 to 176      ; 0              ; -162 to 171       ; 666             ;
; 52     ; -168 to 168      ; 3              ; -162 to 171       ; 667             ;
; 53     ; -180 to 184      ; 10             ; -171 to 171       ; 667             ;
; 54     ; -180 to 184      ; 4              ; -189 to 198       ; 666             ;
; 55     ; -176 to 176      ; 0              ; -144 to 153       ; 665             ;
; 56     ; -176 to 176      ; 7              ; -171 to 171       ; 671             ;
; 57     ; -176 to 180      ; 21             ; -162 to 162       ; 677             ;
; 58     ; -180 to 184      ; 10             ; -162 to 171       ; 678             ;
; 59     ; -192 to 196      ; 21             ; -162 to 162       ; 680             ;
; 60     ; -184 to 184      ; 10             ; -144 to 153       ; 675             ;
; 61     ; -196 to 200      ; 15             ; -153 to 153       ; 681             ;
; 62     ; -188 to 192      ; 0              ; -153 to 162       ; 669             ;
; 63     ; -184 to 184      ; 21             ; -153 to 162       ; 679             ;
; 64     ; -176 to 176      ; 14             ; -171 to 180       ; 637             ;
; 65     ; -172 to 176      ; 6              ; -162 to 171       ; 634             ;
; 66     ; -172 to 176      ; 4              ; -162 to 162       ; 631             ;
; 67     ; -164 to 168      ; 7              ; -189 to 189       ; 635             ;
; 68     ; -164 to 168      ; 12             ; -171 to 171       ; 636             ;
; 69     ; -164 to 168      ; 0              ; -162 to 162       ; 634             ;
; 70     ; -184 to 184      ; 14             ; -180 to 180       ; 637             ;
; 71     ; -180 to 180      ; 10             ; -171 to 180       ; 636             ;
```

+--------+-----------------+---------------+------------------+-----------------+

DQS Pin Margins Observed During Calibration					
DQS Pin	DQS Read Margin (ps)	DQS Input Delay	DQS Write Margin (ps)	DQS Output Delay	DQS Enable Delay
0	-168 to 172	66	-153 to 162	599	1586
1	-180 to 180	69	-144 to 153	633	1587
2	-168 to 168	64	-144 to 153	583	2053
3	-168 to 172	75	-144 to 153	656	2129
4	-156 to 160	63	-144 to 153	685	2154
5	-168 to 172	72	-144 to 153	755	2228
6	-156 to 160	63	-144 to 153	703	2183
7	-176 to 176	85	-144 to 153	715	2217
8	-164 to 168	67	-144 to 153	667	2147

FIFO Settings		
Group	VFIFO Setting	LFIFO Setting
0	0	25
1	0	25
2	0	29
3	0	29
4	0	29
5	0	29
6	0	29
7	0	29
8	0	29

Latency Observed During Calibration	
Type	Latency
Read	13
Write	4

Address/Command Margins Observed During Calibration		
Pin	Margin (ps)	Delay Setting
CKE_0	Uncalibrated	1933
CKE_1	n/a	n/a
CKE_2	n/a	n/a
CKE_3	n/a	n/a
ODT_0	Uncalibrated	1933
ODT_1	n/a	n/a
ODT_2	n/a	n/a
ODT_3	n/a	n/a
RESET	Uncalibrated	1933
ACT	-612 to 603	1932
CS_0	-540 to 540	1933
CS_1	n/a	n/a
CS_2	n/a	n/a
CS_3	n/a	n/a
C_0	n/a	n/a
C_1	n/a	n/a

C_2	n/a	n/a
BA_0	-594 to 585	1918
BA_1	-585 to 576	1913
BG_0	-585 to 585	1915
BG_1	-594 to 585	1921
ADD_0	-603 to 594	1915
ADD_1	-594 to 594	1916
ADD_2	-585 to 585	1922
ADD_3	-612 to 612	1919
ADD_4	-612 to 603	1916
ADD_5	-603 to 603	1915
ADD_6	-594 to 585	1914
ADD_7	-603 to 594	1918
ADD_8	-612 to 603	1915
ADD_9	-594 to 585	1911
ADD_10	-576 to 576	1922
ADD_11	-603 to 603	1912
ADD_12	-585 to 585	1919
ADD_13	-594 to 594	1911
ADD_14	-594 to 594	1921
ADD_15	-612 to 603	1934
ADD_16	-603 to 594	1911
ADD_17	n/a	n/a
ADD_18	n/a	n/a
ADD_19	n/a	n/a
PAR_IN	-603 to 603	1918
ALERT0_N	n/a	n/a
ALERT1_N	n/a	n/a
CK0	n/a	n/a
CK0_N	n/a	n/a
CK1	n/a	n/a
CK1_N	n/a	n/a
CK2	n/a	n/a
CK2_N	n/a	n/a
CK3	n/a	n/a
CK3_N	n/a	n/a

VREF Margins Observed During Calibration

Group	VREFIN margin	VREFIN setting	VREFOUT margin	VREFOUT setting
0	n/a	n/a	n/a	n/a
1	n/a	n/a	n/a	n/a
2	n/a	n/a	n/a	n/a
3	n/a	n/a	n/a	n/a
4	n/a	n/a	n/a	n/a
5	n/a	n/a	n/a	n/a
6	n/a	n/a	n/a	n/a
7	n/a	n/a	n/a	n/a
8	n/a	n/a	n/a	n/a