UNB2_TB_220
Board Description

	Organisatie / Organization	Datum / Date
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Goedkeuring / Approval: A.W. Gunst	Astron	

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1 Introduction

UNB2_TB_220 is part of the UniBoard^2 project which is a Joint Research Activity (JRA) in the RadioNet3 project RD-1, funded by the EC through the FP7 programme, under grant agreement no. 283393. The partners in this JRA are the Universities of Bordeaux and Orleans, INAF, MPG Bonn, the University of Manchester, ASTRON and JIVE. UNB2_TB_220 will be used to test high-speed backplane interfaces of UniBoard^2 and functions as interface board in the housing. The size is UNB2_TB_220 is chosen such that UNB2_TB_220 can be replaces with HEM, HMC Extension Modules to test HMC as memory device for FPGA applications. This document will describe the functionality of UNB2_TB_220

1.1 Reference documents (RD)

Reference document which can be found on
http://www.radionet-eu.org/radionet3wiki/doku.php?id=jra:uniboard2:documents (ask for more details about the wiki Arpad Szomoru, szomoru@jive.nl)

Ref.nr.	Document number	Title
RD-1	RadioNet3 283393	UniBoard2 Work Package description, Arpad Szomoru
RD-2	ASTON-TN-040 1.0	Deliverable 8.2, UniBoard^2 Hardware Design Document

2 Board description

In Table 1 and overview of the connectors placed on UNB2_TB_220 is shown.

Table 1 Overview UNB2_TB_220 connectors

Refdes	Function	Refdes	Function
P1_0, P2_0	High-speed backplane to node 0	P3	Clock input
P1_1, P2_1	High-speed backplane to node 1	P4	PPS input
P1_2, P2_2	High-speed backplane to node 2	P5	Power input
P1_3, P2_3	High-speed backplane to node 3	P15	JTAG
P7-14	Test Connectors	J1	UniBoard^2 ON/OFF
P16-19	Fan connector		

In the following subsection the location and the functionality of the connectors are described in more details.

2.1 Power entry

In Figure 1 an overview of UNB2_TB_220 is given. In this picture the power entry connector is shown.

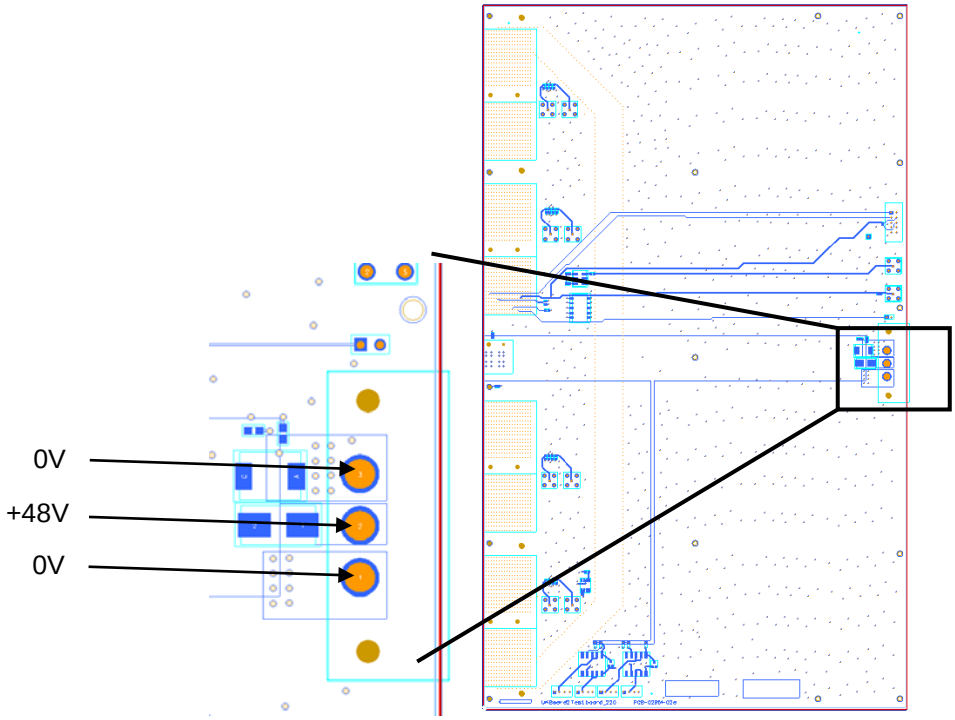

Figure 1 48V Power Entry

48V input remark: UniBoard^2 has an isolated 48V power input. This means that a positive 48V power supply should be connected with the +48V-connection to the pin in the middle of connector P5 and the GND-connection to the left and right pins of P5.

2.2 UniBoard^2 ON/OFF jumper

On UNB2_TB_220 a jumper/connector is placed to enable ON/OFF functionality. In Figure 2 the location of this jumper is shown. By placing a short between the two pins, UniBoard^2 is placed in standby mode.

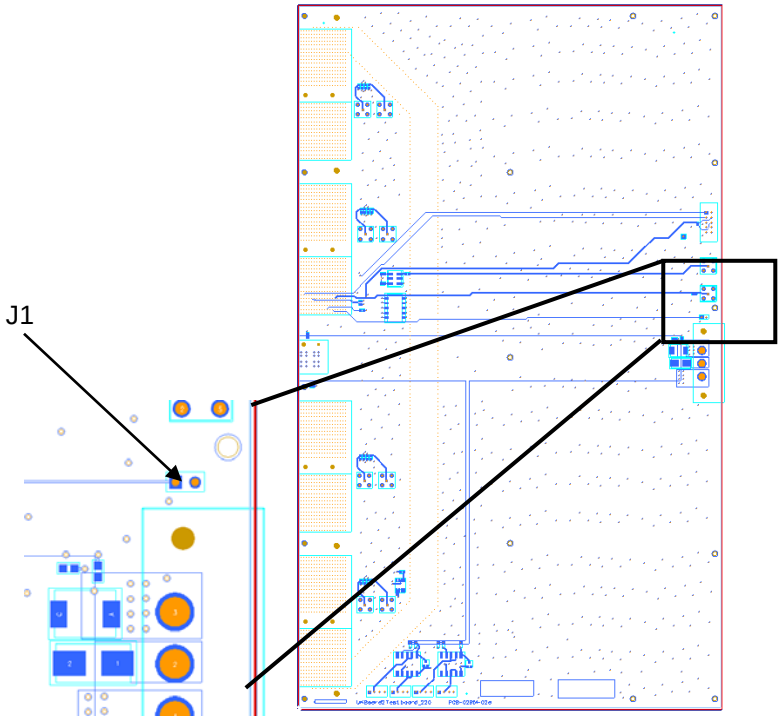

Figure 2 Location of UniBoard² ON/OFF jumper

2.3 CLK and PPS-input

The location of the CLK and PPS inputs are shown in Figure 3. Depending on the jumper setting of UniBoard2 an external clock can be connected to UniBoard2. This clock can be AC-coupled. The range should be 0.5-1.5Vpp, the frequency is dependent on the firmware image. For the pulse per second input (PPS) a simple pulse generator like the Agilent 33250A can be used. The setting depends on the firmware used. For the test image a pulse with an edge time of 5ns, a pulse width of 5ms and a period of 1s can be used. This pulse generator can be locked to the clock through the 10MHz reference input.

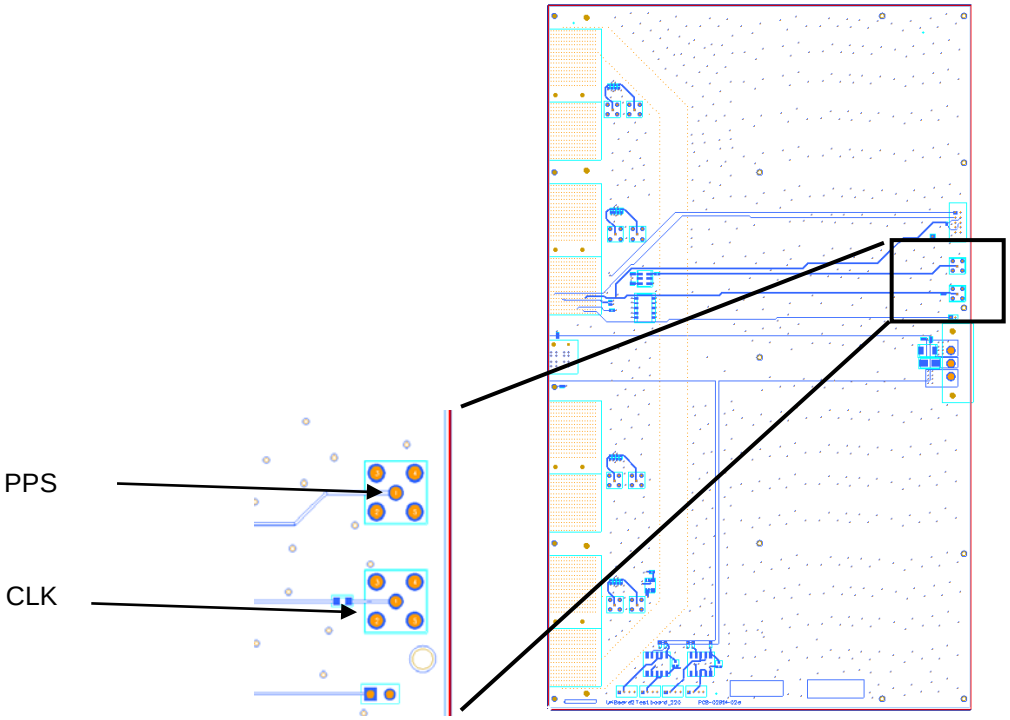

Figure 3 Location of PPS and CLK inputs

2.4 UniBoard^2 ID

Depending on the firmware an external ID can be used for example the Ethernet IP/MAC. In Figure 4 the location of the dip-switch is shown.

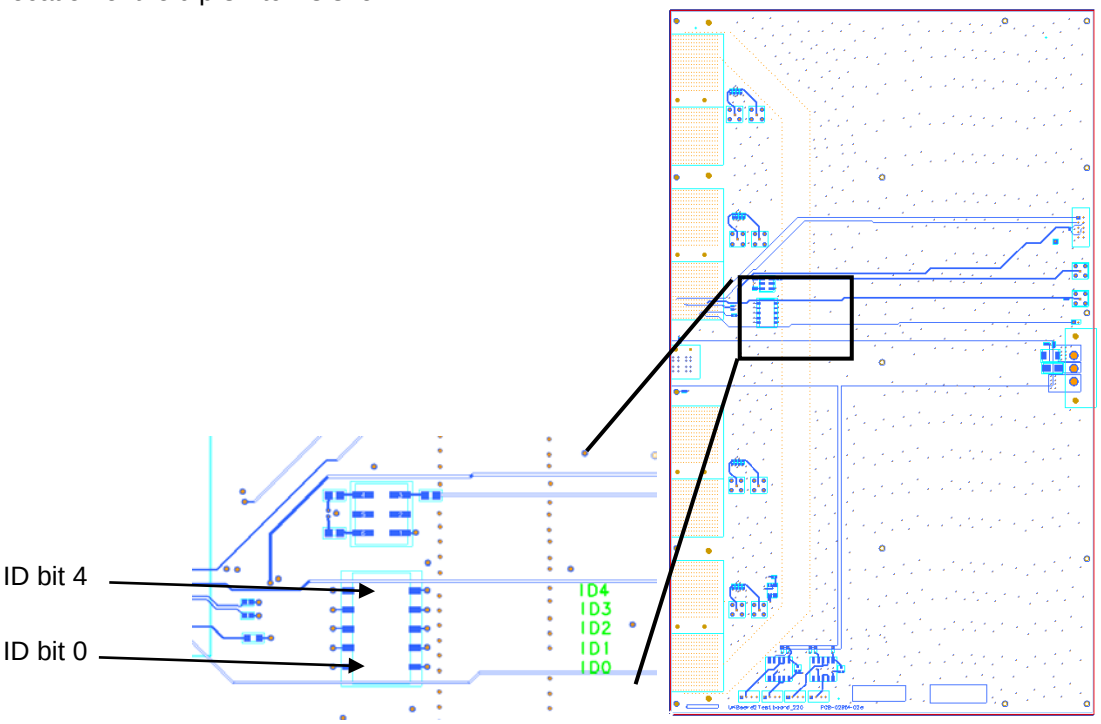

Figure 4 Location of Board ID

2.5 JTAG input

In Figure 5 the JTAG input is shown. The pinning of this connector corresponds with the pinning of the Altera USB-BlasterII. In this way the Altera tools can be used to configure the FPGAs on UniBoard^2.

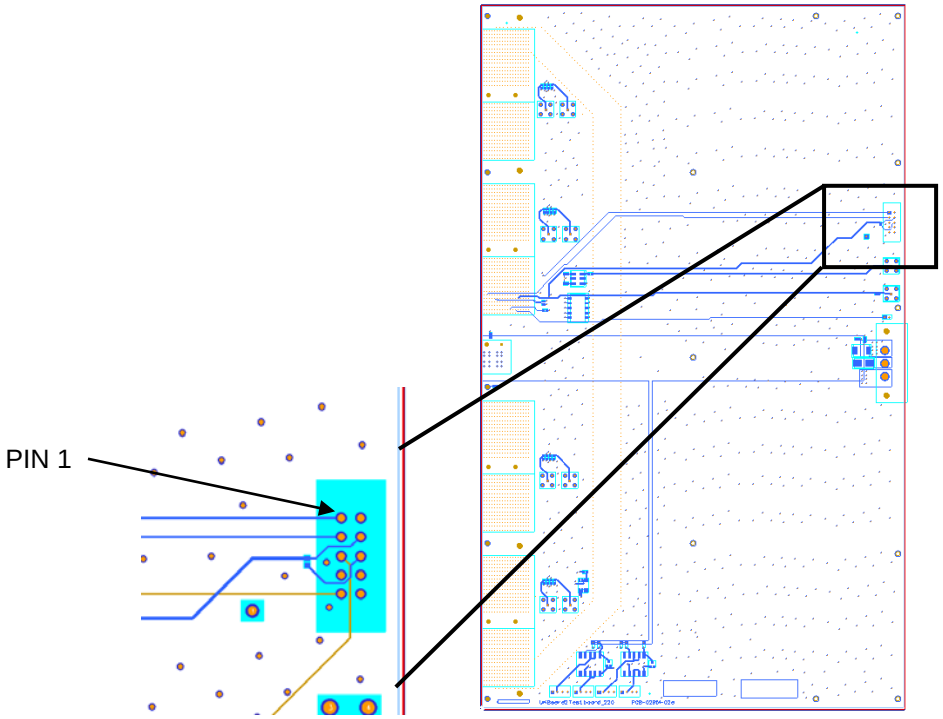

Figure 5 JTAG input

2.6 Fan connectors

On UNB2_TB_220 four identical fan connectors are placed. The FANs are controlled by relays on UNB2_TB_220. When UniBoard2 is placed in low power mode the FANs are switched off. For normal operation all jumpers should be placed.

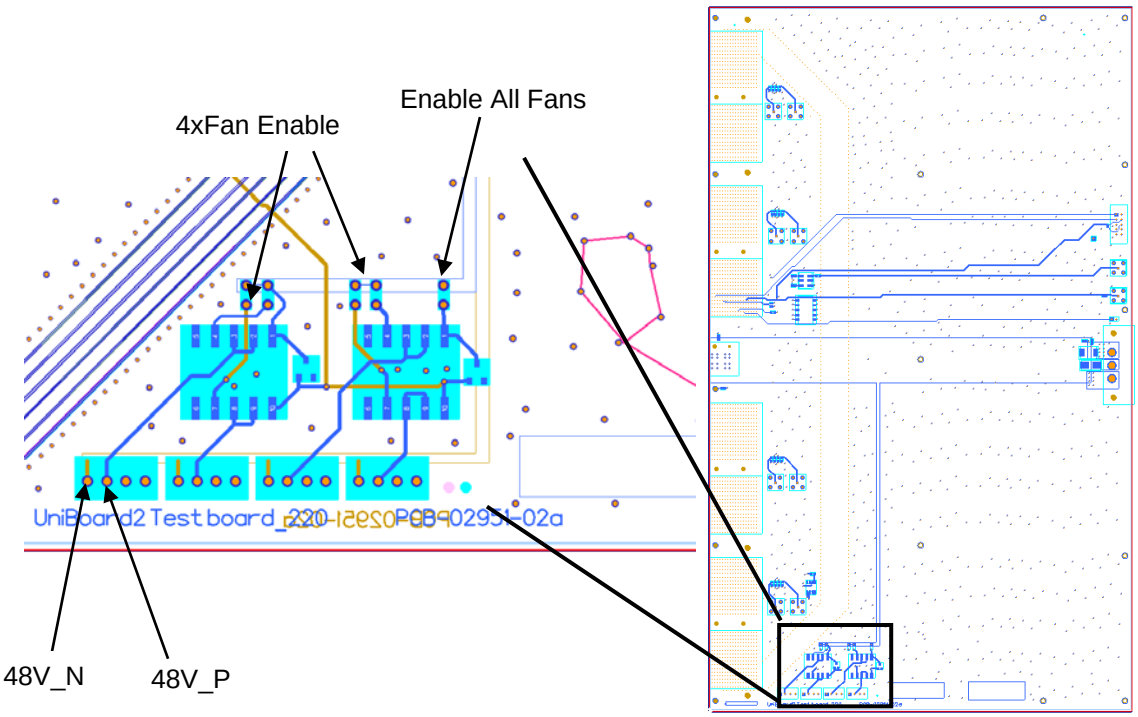

Figure 6 Fan connectors

3 High-Speed test

In Figure 7 an overview of the high-speed traces on layer 8 are shown. On UNB2_TB_220 four high-speed layers are used to closing of the ring interface (long traces) and the short feedback traces on the backplane side.

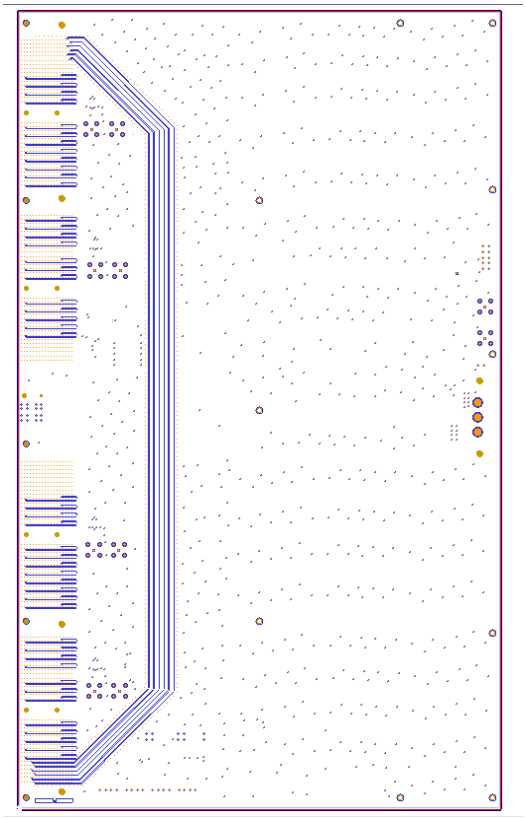

Figure 7 High-Speed traces on layer 8

On every FPGA node connection two SMA connectors are placed to measure the output signal from the FPGA. In Figure 8 the configuration is shown. Normally the resistor are placed, bypassing the connectors. By rotation the resistor 90° the connectors can be used to measure the serial data stream.

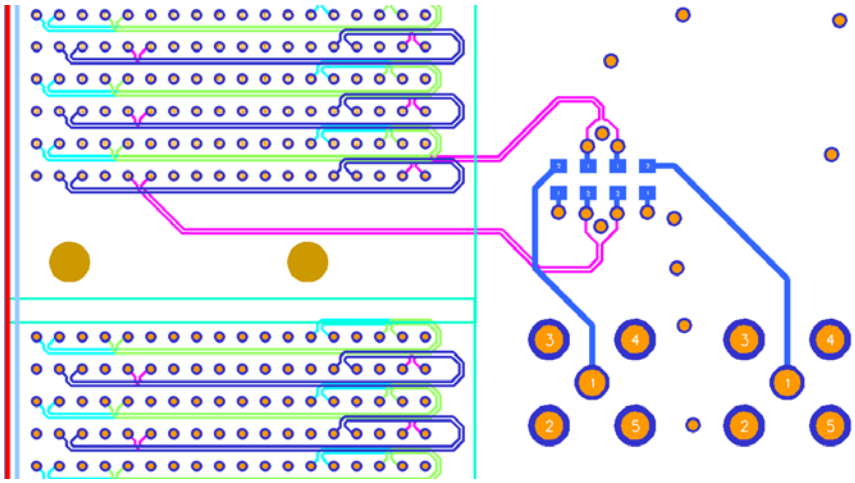

Figure 8 SMA Test connectors

4 Housing

The size of HEM (220mmx366mm) is chosen such that UNB2_TB_220 can be replaced by HEM where the same 2HE housing can be used. In Figure 9 a diagram of the housing is shown.

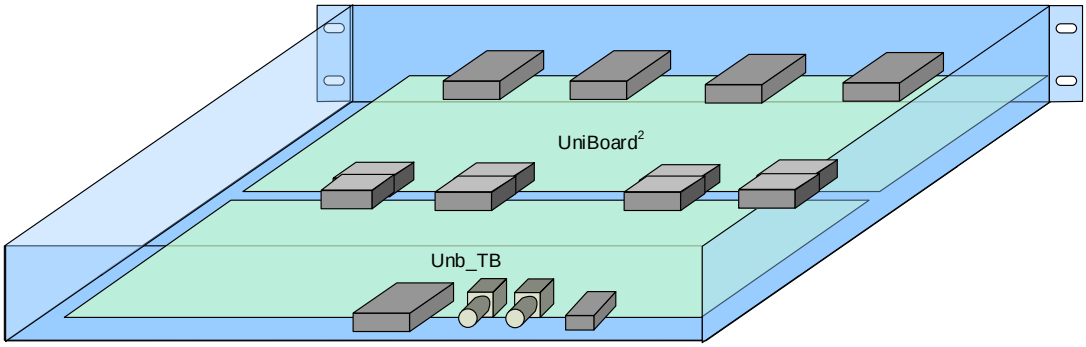

Figure 9 UniBoard2 / UNB2_TB combination in a flat case

5 Pictures of UNB2_TB_220

In Figure 10 and Figure 11 images of UNB2_TB_220 are shown.

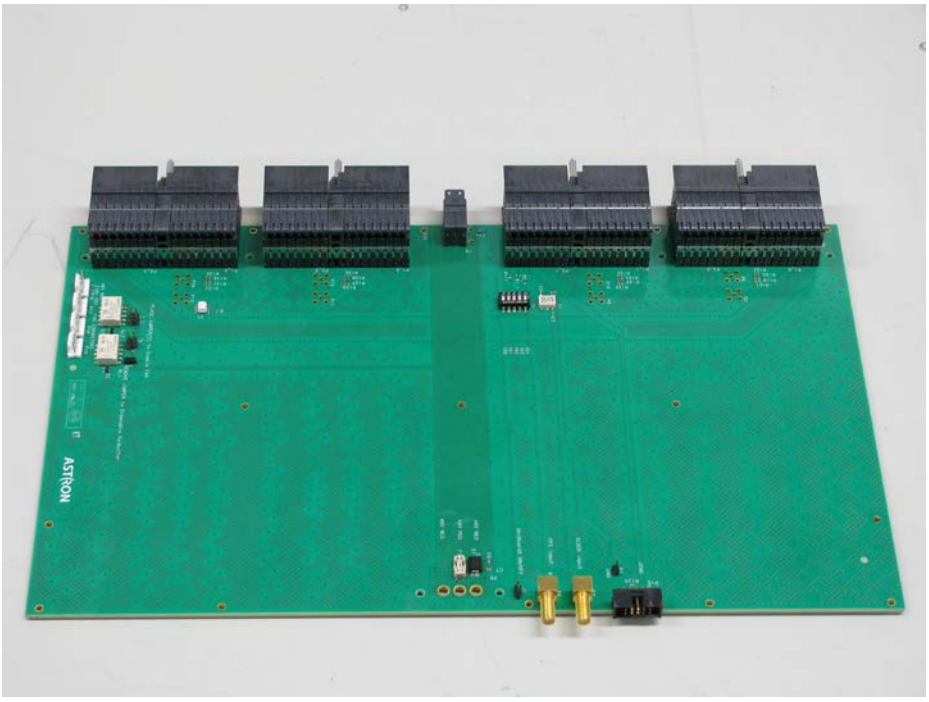

Figure 10 UNB2_TB_220

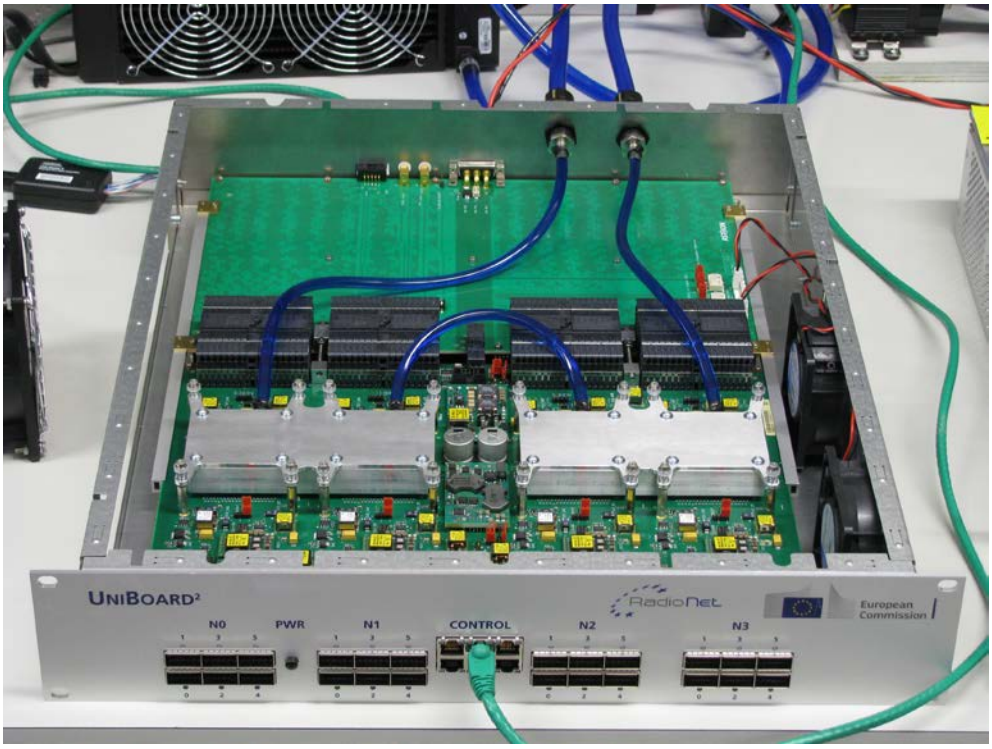

Figure 11 UNB2_TB_220 connected to UniBoard²