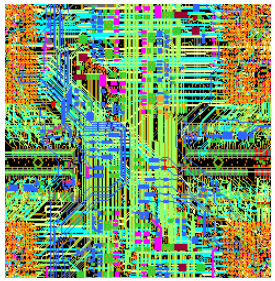
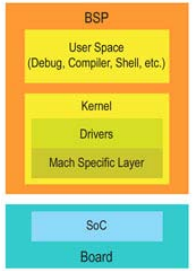
Local parallel (12) optical interface

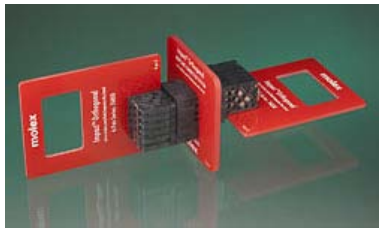
Liquid cooling



Copper mesh @ 14Gbps



on chip Processor

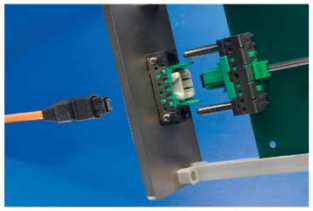


Orthogonal backplane interface

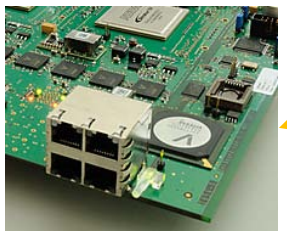
QSFP+ 2x4x10/25Gbps

Stratix VI 20nm FPGA

DDR4 SODIMM

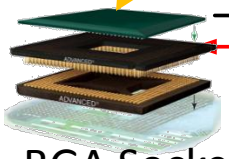


Optical interface

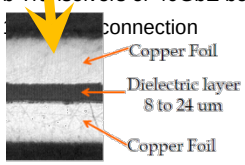


On board 1GbE switch

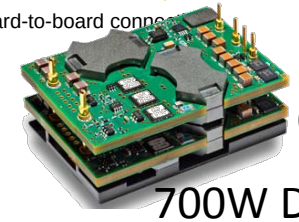
Green Assembly



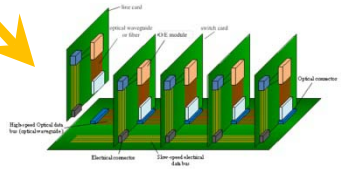
BGA Socket



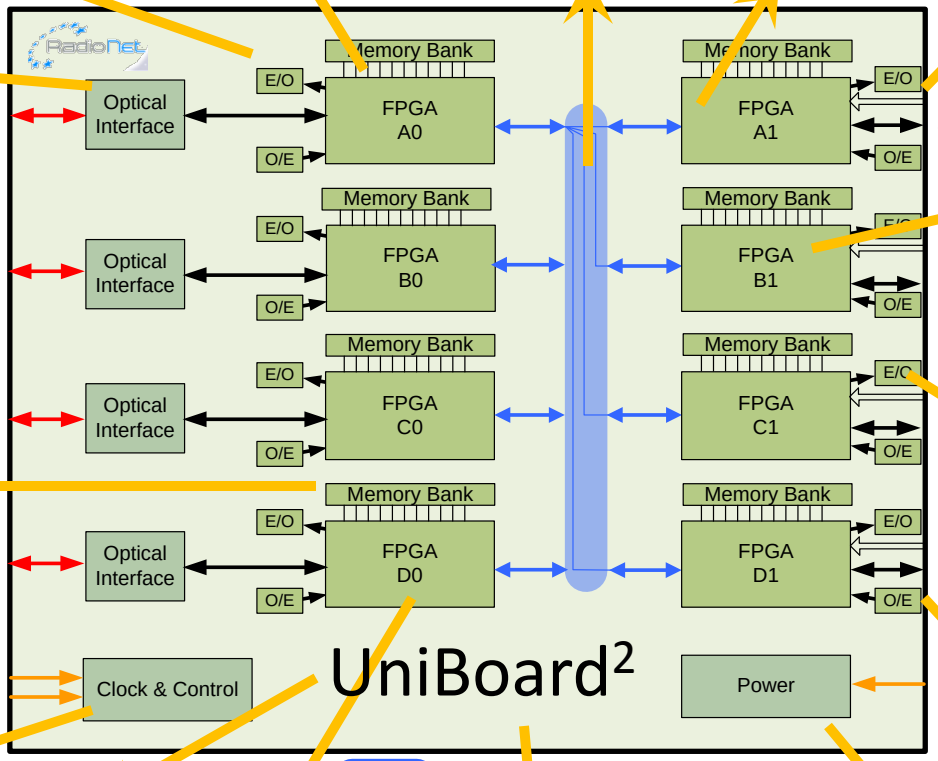
Embeded passives



700W DC/DC



Optical backplane



Mesh between all input and all output fpga's

multi x Gb Transeiver fpga-to-fpga connection

Multi Gb Transeivers or 40GbE board-to-board connection

multi x 1 connection

UniBoard^2 Specifications

- 800Gbps QSFP+ IO at front panel
  - Optic 4x10Gbps (40GBASE-SR4) / 4x25Gbps
  - Direct attach copper (up to 40Gbps)
- 400Gbps copper interface at rear side
- Mesh back to front nodes (bundles of 4 pairs each pair 14Gbps)
- Extra Parallel Optic 12x10Gbps per FPGA for:
  - Optical backplane
  - Full XY mesh between FPGA
  - Extra front panel IO adding 960 Gbps
  - PCIe to PC (can be used for testing OpenCL)
  - Optical ADC interface (120Gbps per FPGA)
- Eight FPGA with:
  - X fixed point multipliers or x floating point multipleirs
  - DDR4 controller in IP (low power)
- Two SODIMM DDR4 memory per FPGA resulting in:
  - 16 Gbyte memory per FPGA
  - 2400MT/s peak performance (total 2400Gbps peak)
- Possible to place FPGA with integrated hard processor.

UniBoard → UniBoard^2

Things to stay the same;

- LVDS interface for ADCs at least 32 pairs @1.2Gbps per FPGA
- Maximal processing power (8 FPGAs)
- Control to FPGA with dedicated 1 GbE interfaces
- X-mesh of 4 copper lanes from a back node to all front nodes

Besides the technology improvements (more multipliers, higher IO bandwidth) some system improvements should be made:

- Improvements on the 48V power input
- Green technology
- 10Gbit interface upgrade to 10G/1G/100BASE-T
- Increase ADC bandwidth on BN
- Increase external memory access
- More test points per FPGA (8 points)
- JTAG bypass

Nice to have are.

- CPU (on module)
- More smaller memory interfaces
- Central board control
- Break out boards with different standards like FMC
- Direct Attachment interfaces for IO
- 72 bits memory interfaces
- Y-mesh from a back node to all other back nodes
- FPGAs in sockets

Thing that can be improved

- FAN control lines

Things that are not needed anymore

- INTA / INTB
- Jumpers next to FPGA