Uniboard2 Architecture Proposal

1 LVDS Interface or Not? List of current High-Performance ADCs

Table I: (Incomplete) List of High-Performance ADCs

Manufacturer / Component / Family	Width [bits]	Sample Rate [GS/s]	BW [GHz]	LVDS Variants	SerDes Variants
Micram ADC-30	6	30	20	0	1
Adsantec ASNT7120-KMA	4	11	18	1	0
Hittite HMCAD5831LP9BE	3	26	20	0	1
Tektronix TADC-1000	8	12.5	8	1	0
e2v EV10Ax	10	1.25 - 5	2.3 - 5	4	0
e2v EV8AQ160	8	1.25 - 5	2	1	0
e2v EV12AS200	12	1.5	2.3	1	0
TI ADC12Dx	12	1 - 3.6	1.2 - 2.8	9	0
TI ADC10Dx	10	2 - 3	1.25 - 2.8	3	0
TI ADC08x	8	1 - 3	1.7 - 3	7	0
TI LM97600	7.6	5	1.2	0	1
TI ADC07D1520	7	1.5, 3	2	1	0
TI ADS42xB69	16	0.25	0.9	1	1
TI ADS41x, ADS42x, ADS44x	14	0.25	0.5 - 0.9	6	1
MAXIM MAX109	8	2.2	2.8	1	0
Analog AD92x, AD96x, AD66x	14	0.15 - 0.25	0.4 - 1	4	4
Analog AD66x, AD94x	12	0.5	1	2	0
Linear div.	10 - 14	0.25 - 0.31	1.2	13	0
Intersil ISLA216x	16	0.13 - 0.25	0.7	3	3
Intersil ISLA214x	14	0.5	0.7	1	1
Sum LVDS / SerDes				59	13

Conclusion: majority of ADCs use LVDS. Often, where there is a SerDes-version, there is also an LVDS-sibling.
The LVDS-signals should be put on a separate connector together with the clock and control lines. For purely backplane-oriented applications, this connector can then be omitted from the board.

2 UNIBOARD MESH

Block diagram in document from Gijs redrawn (without HMC and general infrastucture).

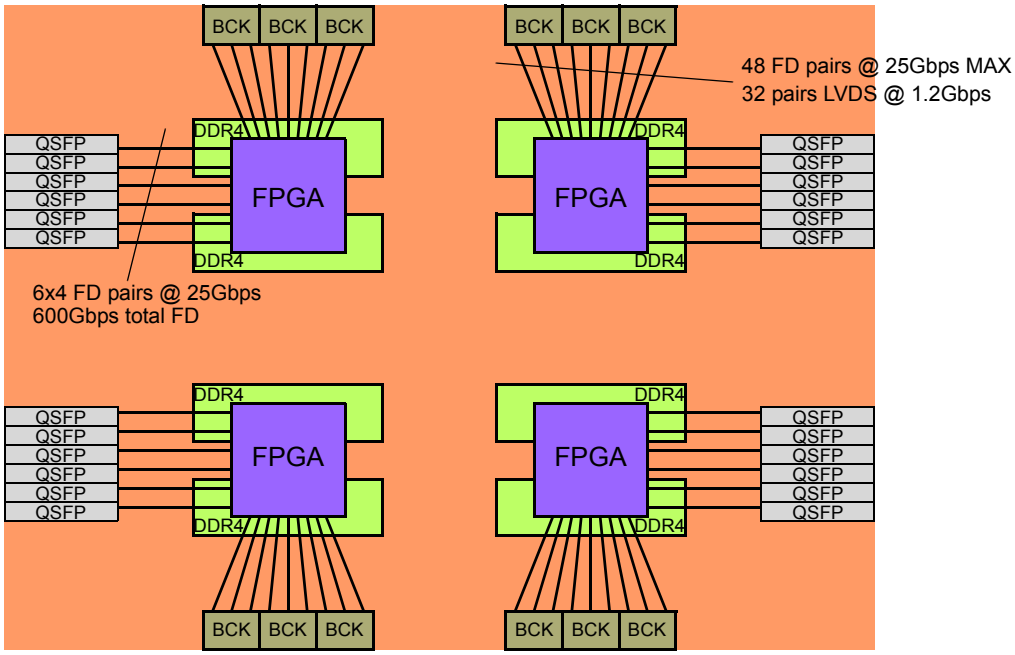

Figure 1: Uniboard2 redrawn

On-board mesh added (assuming 96 transceivers per chip).

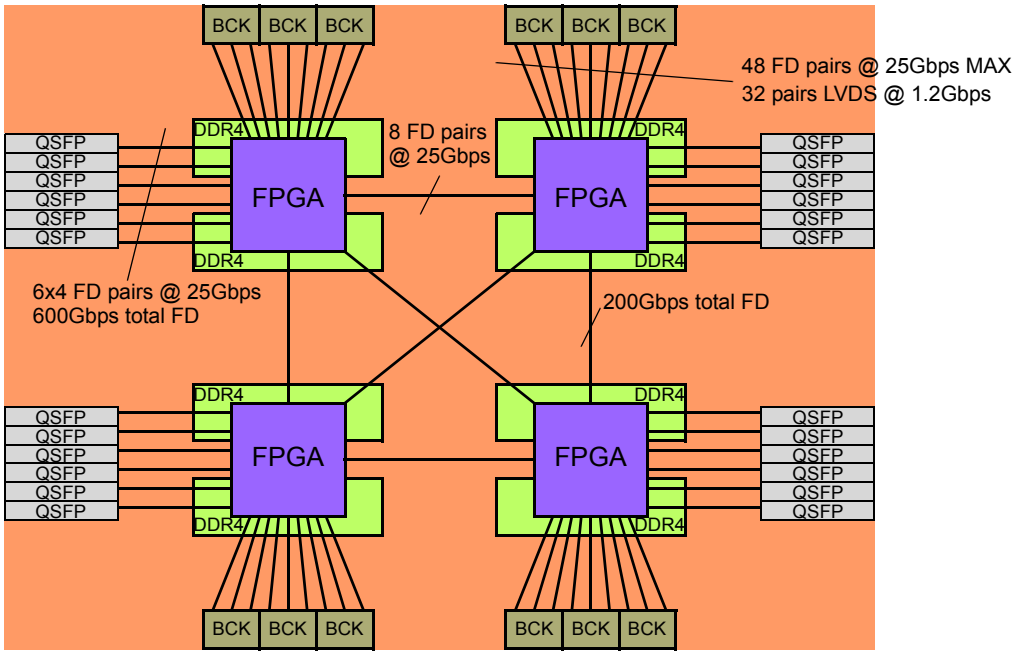

Figure 2: On-board Mesh added

FPGAs conceptually divided into FNs and BNs.

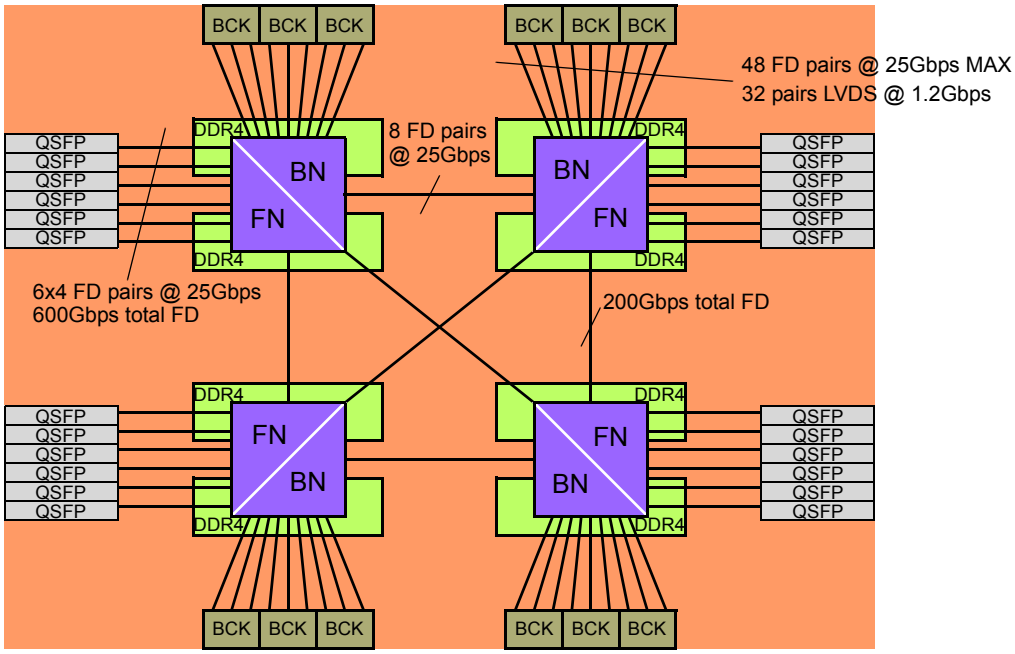

Figure 3: Functional Division

Redrawn as virtual Uniboard1-architecture (memory omitted). Mesh is only unidirectional, which is okay for digital receivers. Chip resources can be arbitrarily allocated between FN and BN. “Single-column”-approach is maintained. Backplane architecture is unaffected.

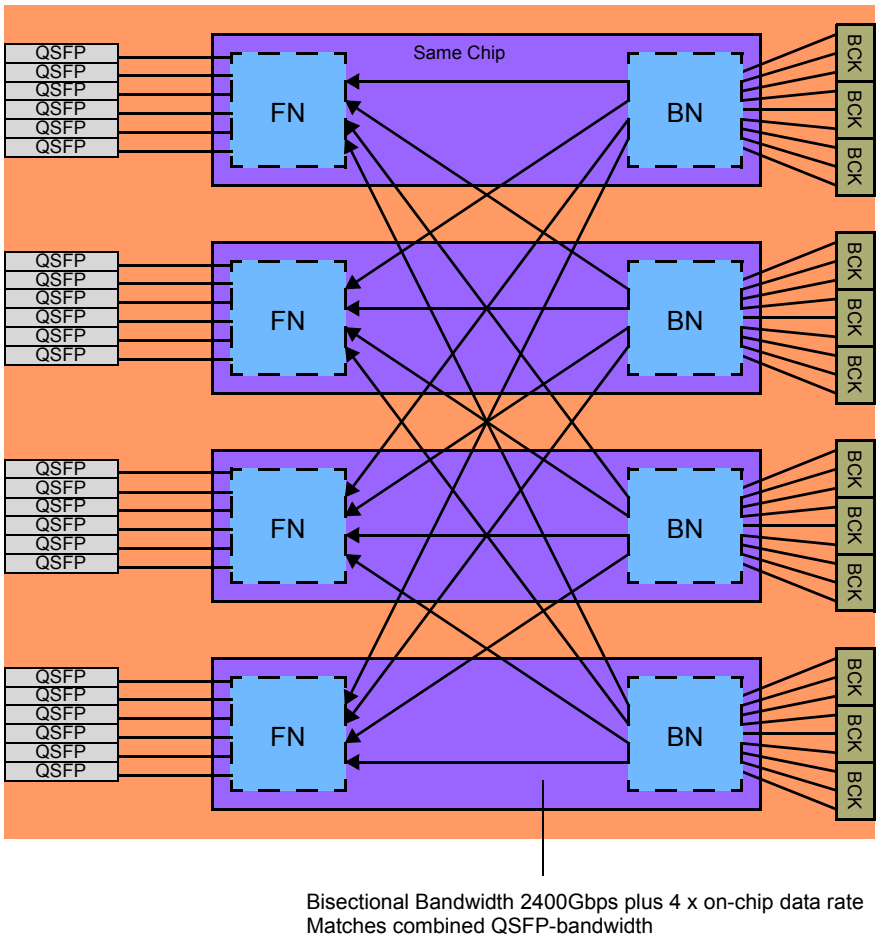

Figure 4: Uniboard2 emulating Uniboard1 (e.g., for Digital Receiver)