Wideband Down-Conversion and Channelisation Techniques for FPGA

Eddy Fry
RF Engines Ltd

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Who are RF Engines?

- Signal processing IP core supplier for FPGA
- SoPC designer of complex optimised front end sub-systems for FPGA
- Signal processing subsystem consultant and supplier, FPGA + DSP
FPGAs vs DSPs
DSP Devices

• Advantages:
  – Moderate performance
  – Easy design methodologies
  – Cheap and easily available
  – Highly flexible

• Disadvantages
  – Moderate performance
FPGA Devices

• Advantages:
  – High performance
  – Re-programmable

• Disadvantages
  – Design methodologies seen as difficult
  – Unit cost can be high
  – Limited internal memory
When is an FPGA appropriate?

- Very high sustained processing rates
  - Digitisation rates >100MHz to > 1GHz are common
  - Real time processing – no ‘gaps’ in data

- Repetitive algorithms such as Down-Conversion and Channelisation are particularly suited
Reducing FPGA ‘Disadvantages’

• Design methodologies improving
  – Availability of high performance IP
  – High-level design entry (System Generator for DSP etc)

• Availability of COTS platforms improving
  – Acqiris, Pentek, Spectrum Signal Processing, Nallatech etc
  – Overall system cost lower than RF / DSP-based

• High bandwidth external memory support
FPGA Device Example

- Manufacturer: Xilinx
- Device: XC2VP100
- No of Logic Cells: 99 216
- No of 18-bit x 18-bit Multipliers: 444
- No of 18Kbit RAMs: 444

- Assuming a 180MHz clock rate, maximum theoretical sustained performance is:
  - 496e9 36-bit additions / second
  - 80e9 18-bit x 18-bit Multiplications per second
  - 360 GByte/s Memory bandwidth, but only ~1MByte storage

- Other manufacturers: Altera, Actel, Lattice etc
External Memory Support

• High bandwidth SRAM (QDR, ZBT etc)
  – 10’s MBytes storage
  – Few GBytes / s bandwidth
  – Random addressing

• High bandwidth SDRAM (DDR etc)
  – Few GBytes storage
  – ~1 GBytes / s bandwidth for block addressing
  – << GBytes / s bandwidth for random addressing
Down-Converter and Channeliser Types
• Digital Down-Converter (DDC)
  – Real to complex conversion (full Nyquist)
  – Narrow-band channel extraction

• Fixed Multi-Channel Down-Converter (Channeliser)
  – FFT
  – Polyphase DFT
  – PFT

• Re-configurable Multi-Channel Down-Converter
  – Tuneable PFT
## Real to Complex DDC Examples

**RFEL’s Distributed Half-Band Filter (DHBF)**

<table>
<thead>
<tr>
<th></th>
<th>DDC #1</th>
<th>DDC #2</th>
<th>DDC #3</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ADC sample rate</strong></td>
<td>200MHz</td>
<td>1GHz</td>
<td>2GHz</td>
</tr>
<tr>
<td><strong>Nyquist input bandwidth</strong></td>
<td>100MHz</td>
<td>500MHz</td>
<td>1GHz</td>
</tr>
<tr>
<td><strong>IF</strong></td>
<td>50MHz</td>
<td>250MHz</td>
<td>500MHz</td>
</tr>
<tr>
<td><strong>Input precision</strong></td>
<td>14-bit real</td>
<td>8-bit real</td>
<td>8-bit real</td>
</tr>
<tr>
<td><strong>Output precision</strong></td>
<td>16-bit complex</td>
<td>9-bit complex</td>
<td>9-bit complex</td>
</tr>
<tr>
<td><strong>Alias-free bandwidth</strong></td>
<td>80MHz</td>
<td>400MHz</td>
<td>800MHz</td>
</tr>
<tr>
<td><strong>Stopband attenuation</strong></td>
<td>95dB</td>
<td>85dB</td>
<td>85dB</td>
</tr>
<tr>
<td><strong>FPGA resource</strong></td>
<td>10% XC2V3000</td>
<td>15% XC2VP70</td>
<td>30% XC2VP70</td>
</tr>
</tbody>
</table>

**Experts in signal processing for FPGA**
FFTs
RFEL’s ‘Vectis’ Pipelined FFTs

Experts in signal processing for FPGA
Experts in signal processing for FPGA

Vectis HiSpeed Architecture

\( n \times \text{radix-2 FFT stages} \)

FFT Length = \( 2^n \)

Interleaved I and Q

Input Buffer (optional)

Stage n

Stage 2

Stage 1

Bit Reverser (optional)

Normally ordered Output

Samples 0, 1, 2, 3...

Bit Reversed Output

Samples 0, 8, 4, 12, 2, 10, 6, 14....

(Sequence From 16-point FFT shown)

Normally Ordered Inputs

Samples 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10.....
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** Vectis QuadSpeed Architecture **

1:2 De-multiplexed I and Q inputs

\[ n \times \text{radix-2 FFT stages} \]

\[ \text{FFT Length} = 2^n \]

Normally ordered Output
Samples 0, 1, 2, 3...

Normally Ordered Inputs
Samples 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10.....

Input Buffer (optional)

Stage \( n \)

Stage 2

Stage 1

Bit Reverser (optional)

Bit Reversed Output
Samples 0, 8, 4, 12, 2, 10, 6, 14.....
(Sequence From 16-point FFT shown)
HyperSpeed Architecture

FFT Length = N x M

Complex Input @ Fs

Processing @ Fs / M

1:M Demux

0, M, 2M, … (N-1)M

N-Point ‘Matrix’ Serial DFT

0, 1, 2, 3, … NM-1

N-Point ‘Matrix’ Serial DFT

0, M, 2M, … (N-1)M

N-Point ‘Matrix’ Serial DFT

M-1 Complex Multipliers

Twiddle-Factors

M-Point Parallel DFT

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HyperLength Architecture

FFT Length = N x M

N-Point HiSpeed FFT
Twiddle Factors
M-Point HiSpeed FFT

FPGA

Normally Ordered Inputs
Samples 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, ...

Interleaved I and Q

Re-order (External RAM)

Re-order (External RAM)

Re-order (External RAM)

Experts in signal processing for FPGA
## FFT Examples

<table>
<thead>
<tr>
<th></th>
<th>HiSpeed</th>
<th>QuadSpeed</th>
<th>HyperSpeed</th>
<th>HyperLength SRAM</th>
<th>HyperLength SDRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Length (complex)</strong></td>
<td>1K</td>
<td>4K</td>
<td>32K</td>
<td>1M</td>
<td>256M</td>
</tr>
<tr>
<td><strong>Input bandwidth</strong></td>
<td>100MHz</td>
<td>400MHz</td>
<td>1GHz</td>
<td>100MHz</td>
<td>10MHz</td>
</tr>
<tr>
<td><strong>Input precision</strong></td>
<td>17-bit</td>
<td>12-bit</td>
<td>9-bit</td>
<td>16-bit</td>
<td>16-bit</td>
</tr>
<tr>
<td><strong>Output precision</strong></td>
<td>27-bit</td>
<td>24-bit</td>
<td>20-bit</td>
<td>32-bit</td>
<td>36-bit</td>
</tr>
<tr>
<td><strong>Twiddle precision</strong></td>
<td>17-bit</td>
<td>18-bit</td>
<td>17-bit</td>
<td>18-bit</td>
<td>18-bit</td>
</tr>
<tr>
<td><strong>Input-buffer</strong></td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Bit-reverser</strong></td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>FPGA resource</strong></td>
<td>20% XC2V3000</td>
<td>50% XC2V3000</td>
<td>75% XC2VP70</td>
<td>55% XC2V3000</td>
<td>50% XC2V3000</td>
</tr>
<tr>
<td><strong>External memory</strong></td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>5 x 38Mbit QDR II</td>
<td>3 x 4GB DDR DIMM</td>
</tr>
</tbody>
</table>
Polyphase DFT and PFT Filter Banks
Polyphase Filter Vs Weighted FFT

- Unweighted FFT Filter Response
- Polyphase DFT Filter Response
- Kaiser Weighted FFT Filter Response

Offset (Hz)

dBc
32-Point FFT Filter Bank

Kaiser Window

Channel Spacing = $F_s / 32$
32-Point Polyphase Filter Bank

Typical Performance

Channel Spacing = $\frac{F_s}{32}$

Superior Cut-Off & Stop-Band Performance
Polyphase DFT Architecture

Rate = \( F_s \)

Delay 1
K samples

Delay 2
K samples

Delay N-1
K samples

Coeffs \( W_0, W_1, W_2, \ldots, W_{K-1} \)

Coeffs \( W_K, W_{K+1}, \ldots, W_{2K-1} \)

Coeffs \( W_{2K}, W_{2K+1}, \ldots, W_{3K-1} \)

Coeffs \( W_{(N-1)K}, W_{(N-1)K+1}, \ldots, W_{NK-1} \)

N*K Window Coeffs \( W_{NK-1} \) thro' \( W_0 \)

K Point Complex FFT

Rate = \( F_s \)

Duplicate Q Channel
# Polyphase DFT Examples

<table>
<thead>
<tr>
<th></th>
<th>PDFT #1</th>
<th>PDFT #2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transform Length (complex)</td>
<td>8K</td>
<td>8K</td>
</tr>
<tr>
<td>Prototype filter length</td>
<td>32K</td>
<td>32K</td>
</tr>
<tr>
<td>Input bandwidth</td>
<td>204.8MHz</td>
<td>409.6MHz</td>
</tr>
<tr>
<td>Input precision</td>
<td>14-bit</td>
<td>14-bit</td>
</tr>
<tr>
<td>Output precision</td>
<td>28-bit</td>
<td>28-bit</td>
</tr>
<tr>
<td>Twiddle precision</td>
<td>18-bit</td>
<td>18-bit</td>
</tr>
<tr>
<td>Filter passband width</td>
<td>25kHz</td>
<td>50kHz</td>
</tr>
<tr>
<td>Filter stopband width</td>
<td>75kHz</td>
<td>150kHz</td>
</tr>
<tr>
<td>Filter ripple</td>
<td>+/- 0.05dB</td>
<td>+/- 0.05dB</td>
</tr>
<tr>
<td>Filter stopband attenuation</td>
<td>85dB</td>
<td>85dB</td>
</tr>
<tr>
<td>Channel sample rate</td>
<td>50kHz (2x bw)</td>
<td>50kHz (1x bw)</td>
</tr>
<tr>
<td>Bit-reverser</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>FPGA resource</td>
<td>60% XC2VP70</td>
<td>65% XC2VP70</td>
</tr>
<tr>
<td>External memory</td>
<td>None</td>
<td>None</td>
</tr>
</tbody>
</table>
PFT Architecture

- Simultaneous outputs of PFT’s with different number of bins / frequency resolutions
- For example: a 256-point PFT with 400 kHz bin width at same time as a 16K-point PFT with 6.25 kHz bin width
- Useful for discriminating in both frequency and time domains
Tuneable PFT Example
Wideband Spectrometer Example

Pair of 8-bit ADCs are accurately clocked 180° apart to give 2GHz effective sample rate

Total Resource Requirements:
- 308 Multipliers
- 306 RAMs
- ~95% of XC2VP70

Wideband DDC (DHBF)

Window

32K-point HyperSpeed FFT

Fixed-point Complex to Floating-point Power

Accumulate Floating-point Power

1GHz Nyquist bandwidth, 800MHz usable bandwidth, centred on an IF of 500MHz

Each ADC’s data is de-multiplexed into 8 x 8-bit busses at 125MHz for interfacing to FPGA

DHBF converts 2GHz real data into 1GHz complex base-band data (DDC Example #3)

Programmable window applied to complex data. 16 Multipliers, 0 RAMs

Programmable floating-point power accumulator (average) Averaging from 1 to 1K frames 64 RAMs

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Questions?