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# A complete approach:

# From InGaAs channel to cryogenic amplifier

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# Contents

- InP HEMT fabrication
- Amplifiers
- A new technology: InAs/AlSb HEMTs
- Conclusions
- Future work

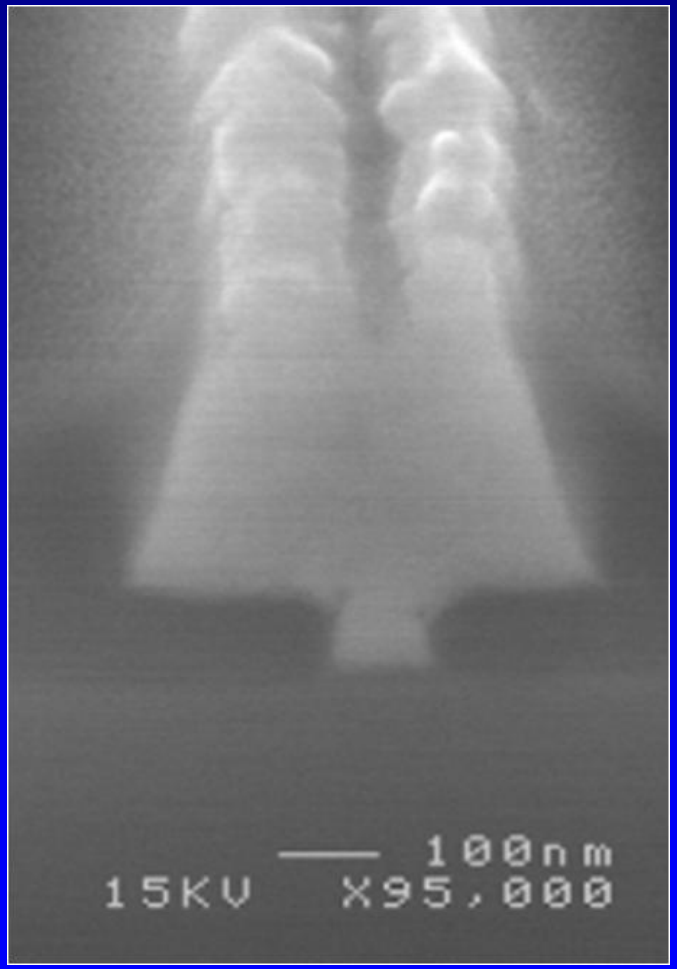
# InP HEMT fabrication

# InP HEMT fabrication

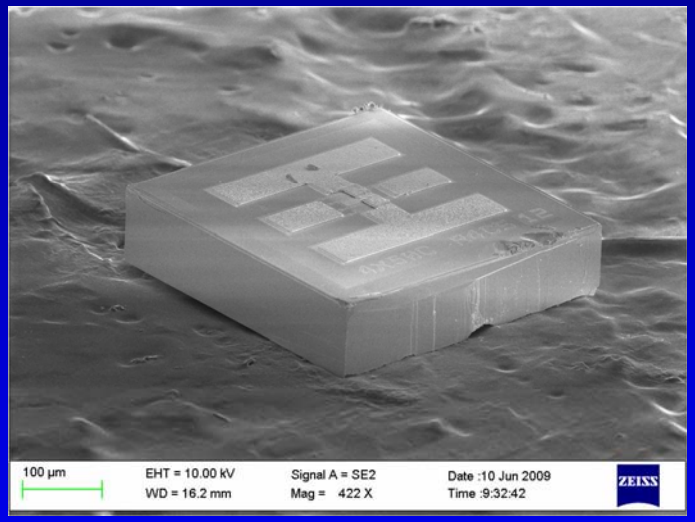

- A complete process flow for InP HEMTs has been set up at the Chalmers NanoFabrication Laboratory
- 2” wafers, Lg = 110 nm
- 8 mask layers

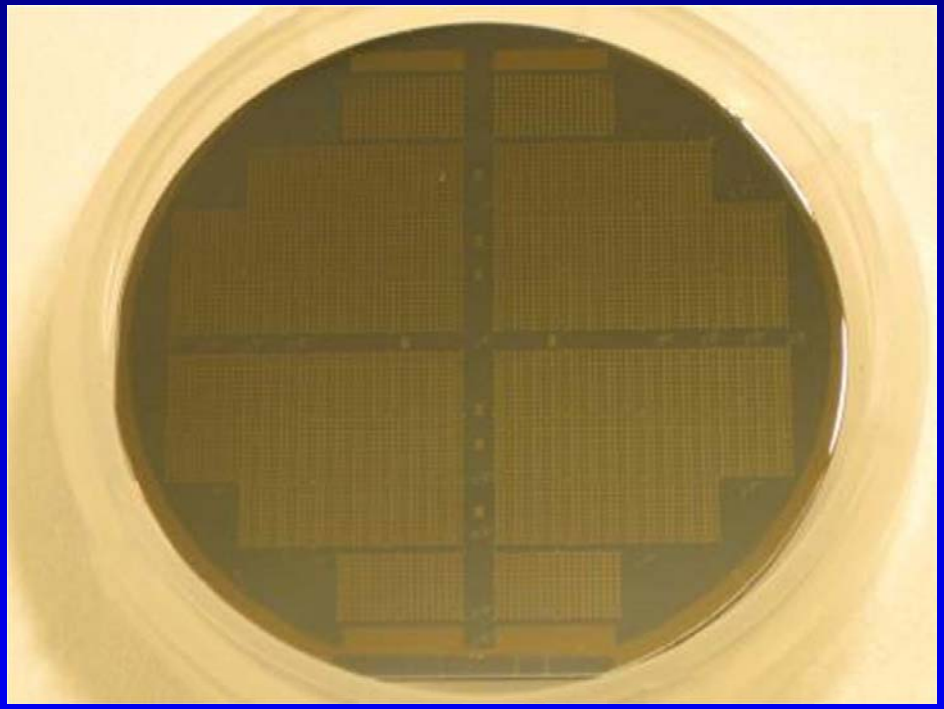
# InP HEMT fabrication

- Mushroom gates, $L_g$ = 110 nm
- Development for 70 nm gates ongoing



# InP HEMT fabrication



- 2” process
- 6000 transistors/wafer

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# Vertical Optimization 130 nm InP HEMT (RT)

DC transconductance

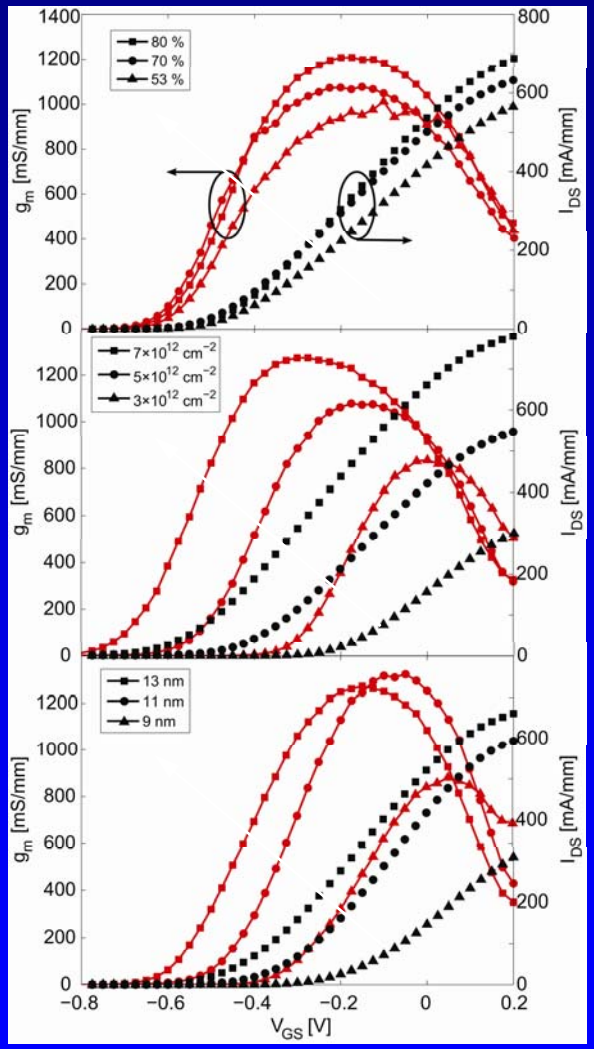
ft/fmax @$V_{DS}$=1.0 V

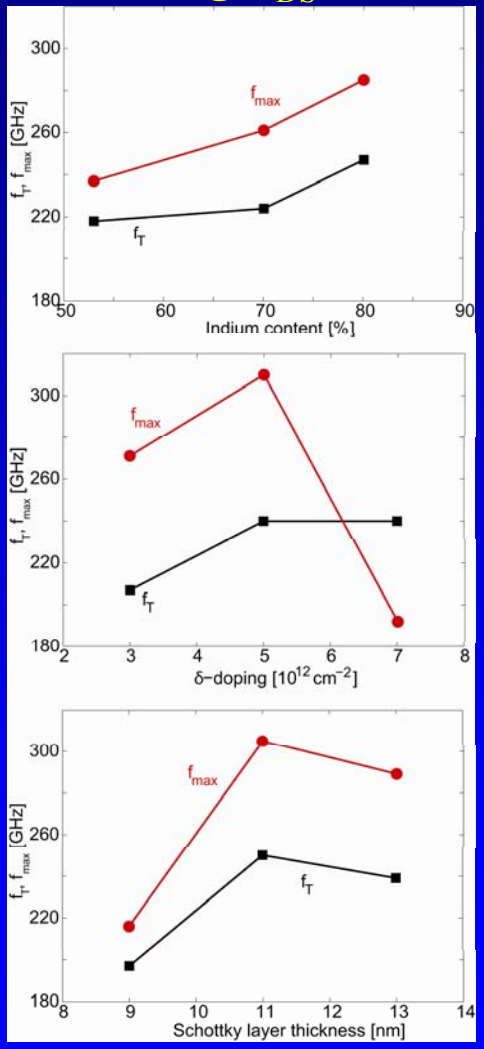
$NF_{min}$@26 GHz

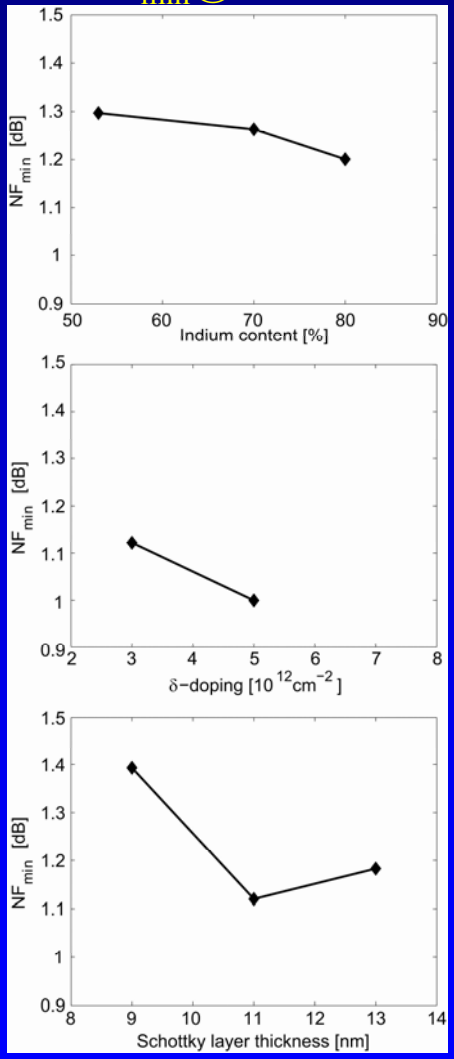
[In]

δ-doping

$d_{SL}$



# HEMT data: Full wafer process

| Parameter | H805 |
|---|---|
| Yield | > 90% |
| Fmax/Ft 2*20µm | 260/150 GHz |
| Fmax/Ft 2*50µm | 240/240 GHz |
| Vbgd | 8.6 V |
| Gm_max | 1000 mS/mm |
| Id_max | 550 mA/mm |
| Ig at typical low noise bias | 10nA |
| Rds_on | 0.85 ohm*mm |
| Cgs at low noise bias | 575 fF/mm |

# Amplifiers

# Specification

| | |
|---|---|
| • Frequency (1 dB band) | 4-8 GHz |
| • Noise temperature | as low as possible |
| • Gain | >35 dB min. |

The specifications are set by ESA/ESOC requirements

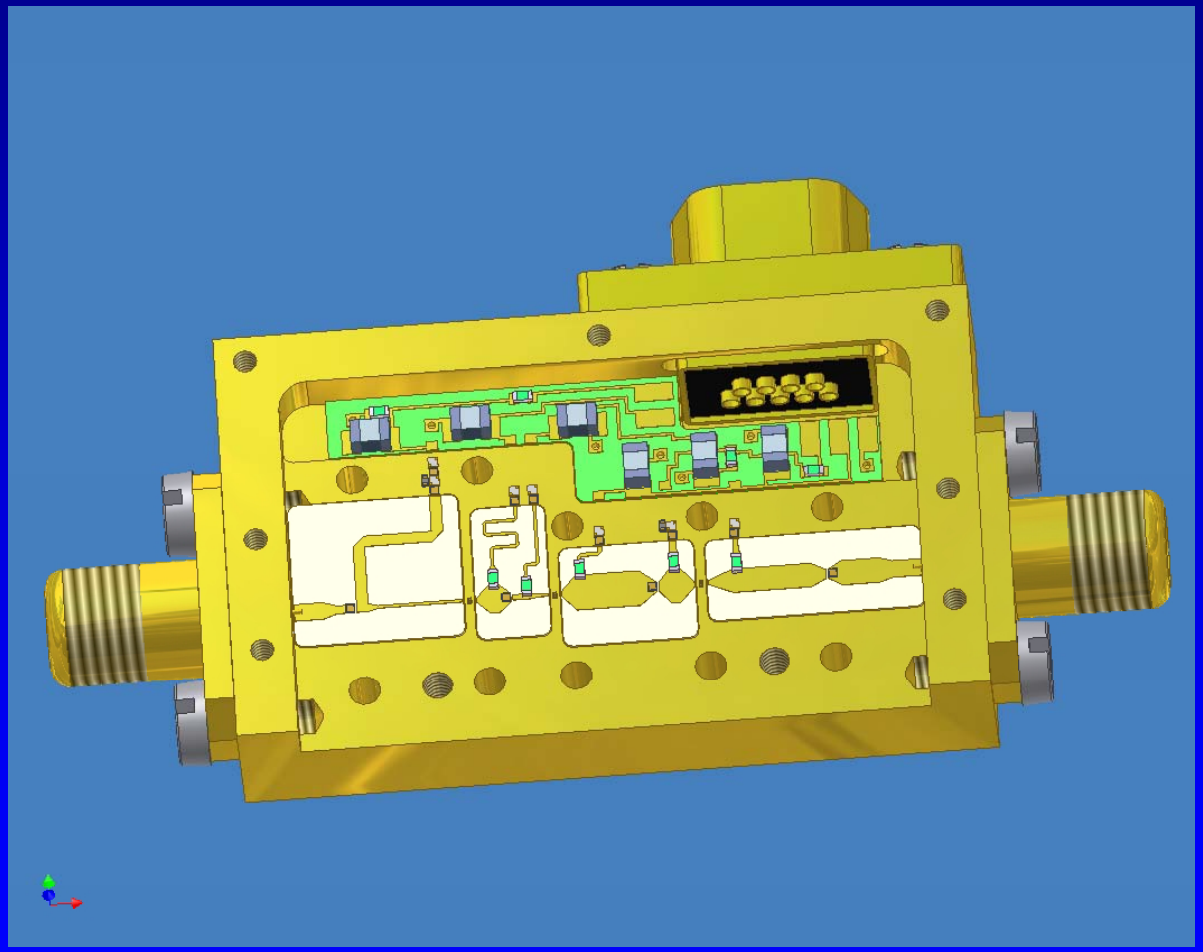
# Active devices

- InP devices manufactured by Chalmers
  - H805, Q4
  - InP35 (pseudomorphic material)
- Cryo 3 by NGST used for comparison

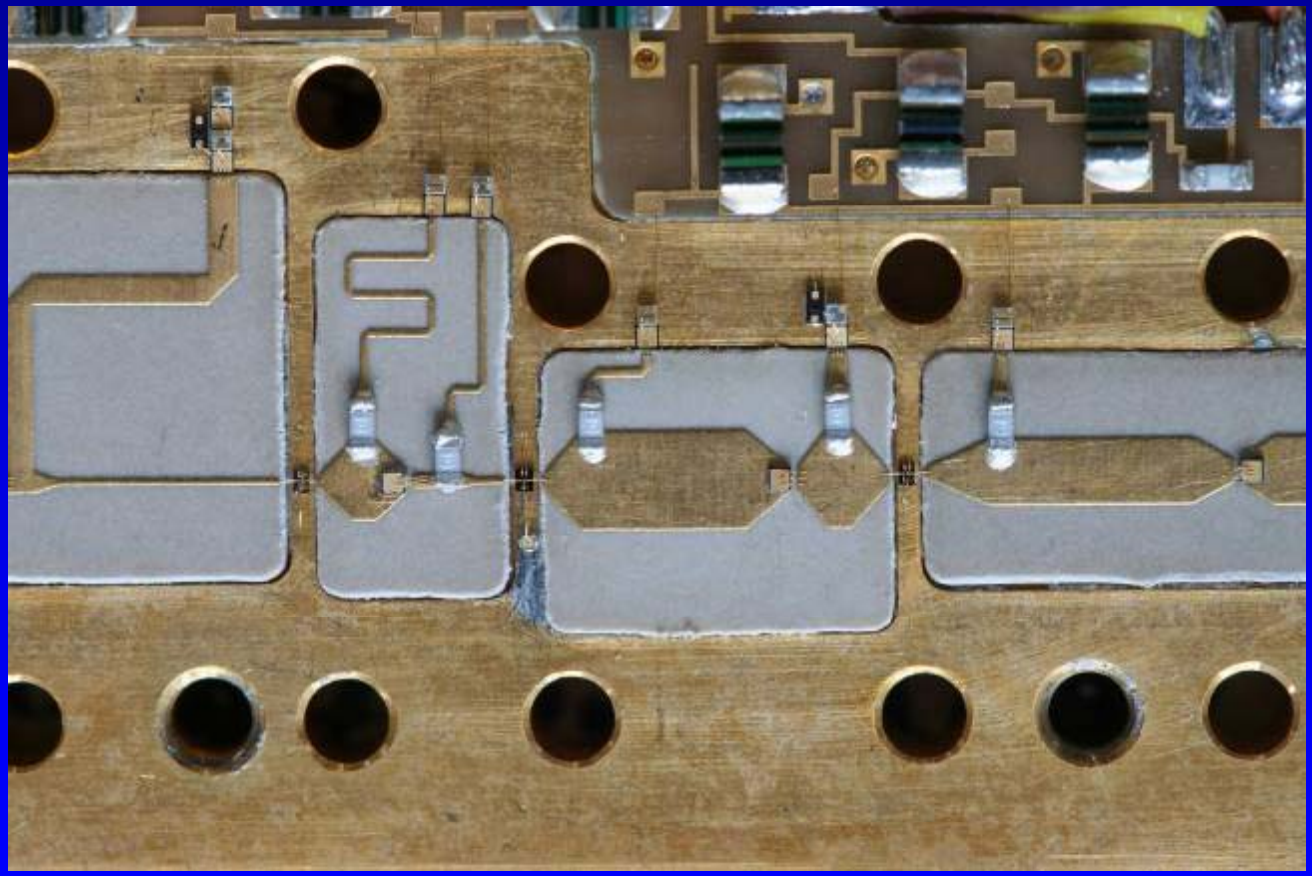
# Substrate

- All amplifiers are designed on RT/duroid 6002 ($\varepsilon_r$=2.94@300K).
- Thickness of the substrate is 0.381 mm (15mil)
- Cu coating, 1/2oz both sides=17.5µm, gold plated (Au 5-8µm, type 3, class A, 90 knoop)

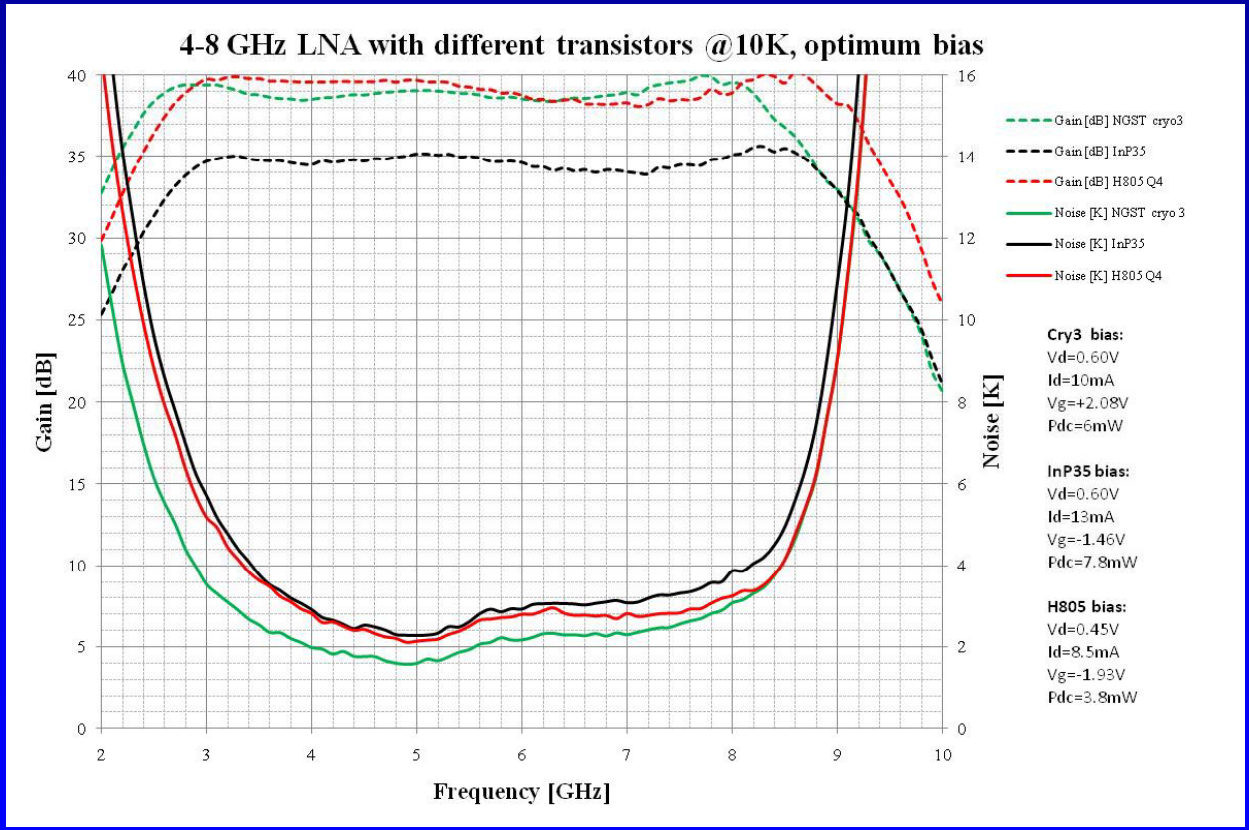
# Assembling



# Photography

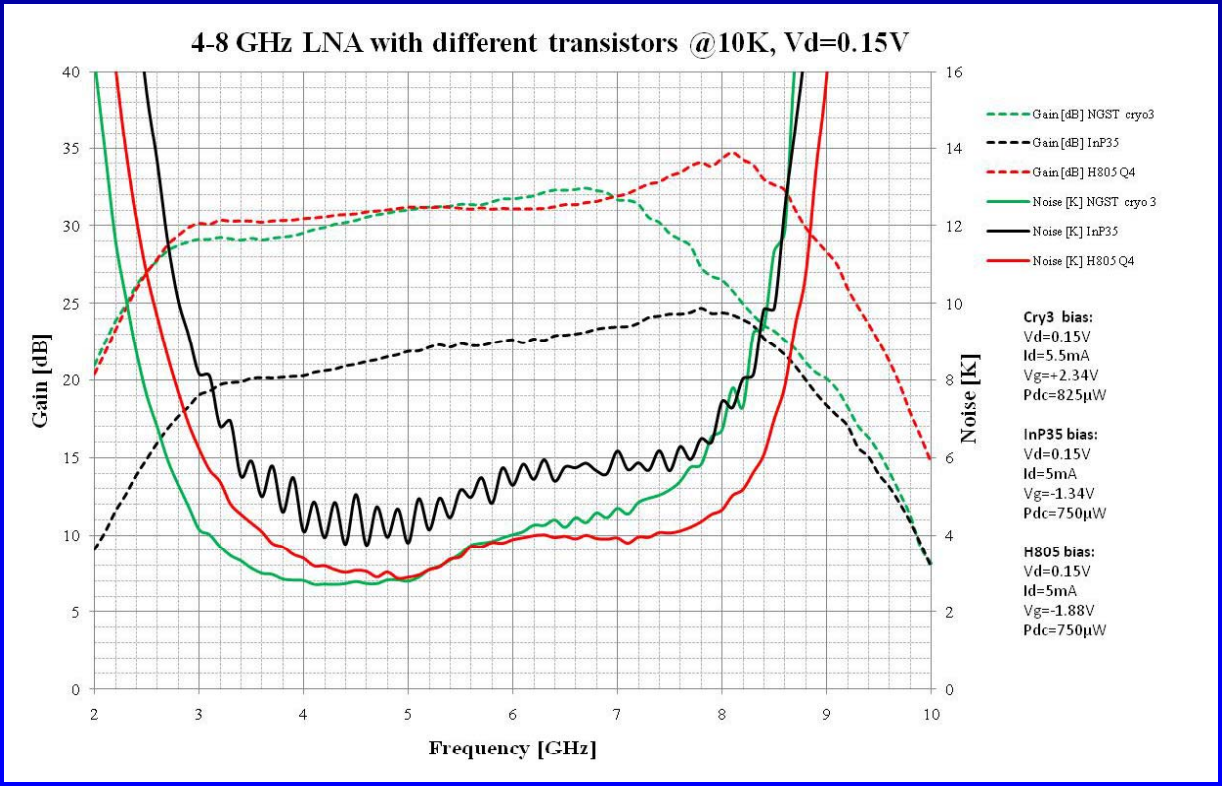


# Measurements
# 10K, optimum bias



# Measurements
# 10K, extremely low bias

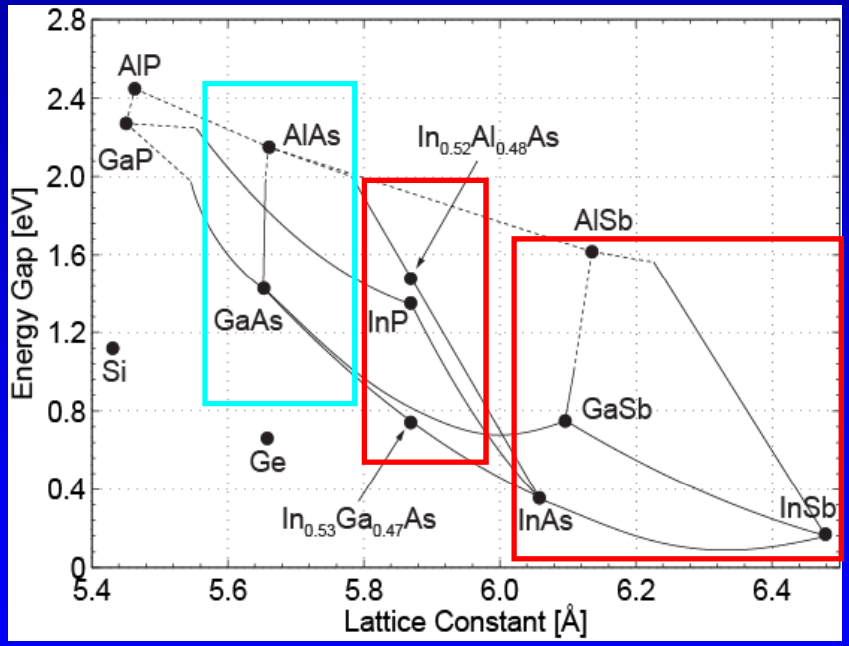


# InAs /AlSb HEMTs: Next generation ultra-low power cryo LNAs?

+ Low DC power consumption
+ $\Delta E_c$
+ High carrier mobility

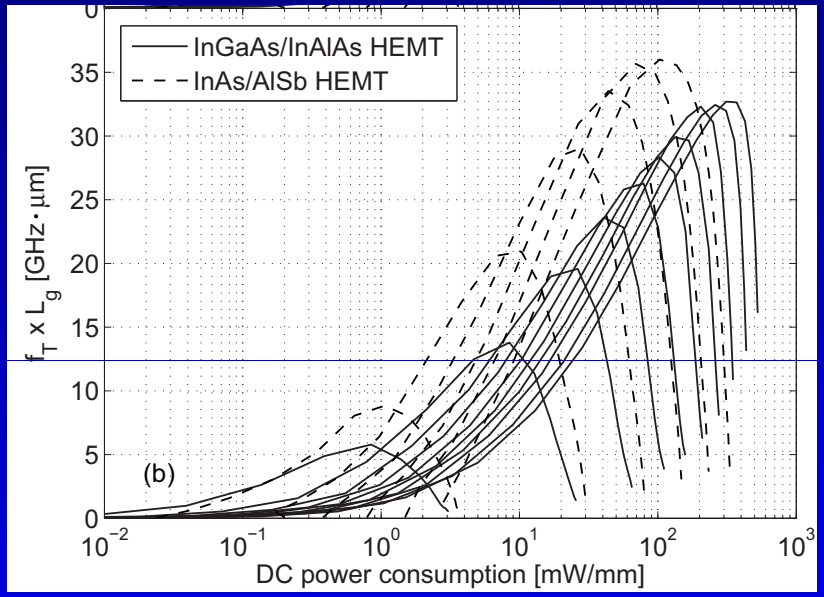
- Immature technology
- Gate-leakage current
- Pinch-off



# Power dissipation and noise: InAs/AlSb HEMT (RT)

225 nm InAs/AlSb HEMT (2x50 um) as a fcn of power dissipation

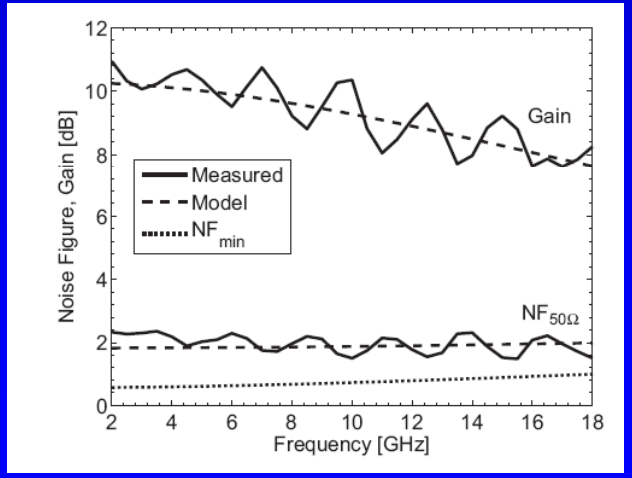
Compard to InP HEMTs:
higher $f_T \times L_g$ product at low $V_{DS}$




Transconductance 650 mS/mm at $V_{DS}$ = 0.2 V

$NF_{min}$ < 1 dB at 2 – 18 GHz at $V_{DS}$ = 0.2 V

Corresponds to DC power consumption of only 10 mW/mm



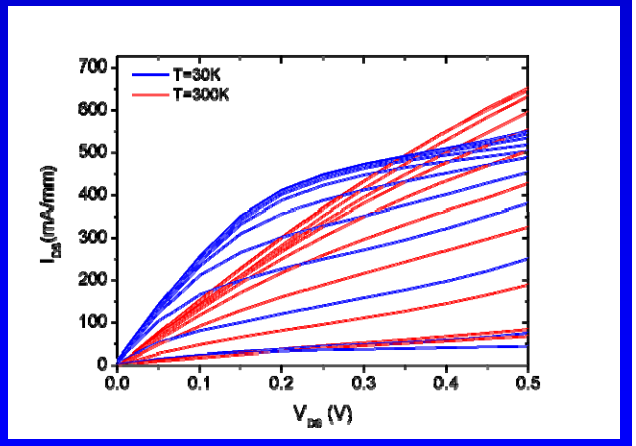
# DC properties: InAs/AlSb HEMTs (30 K)

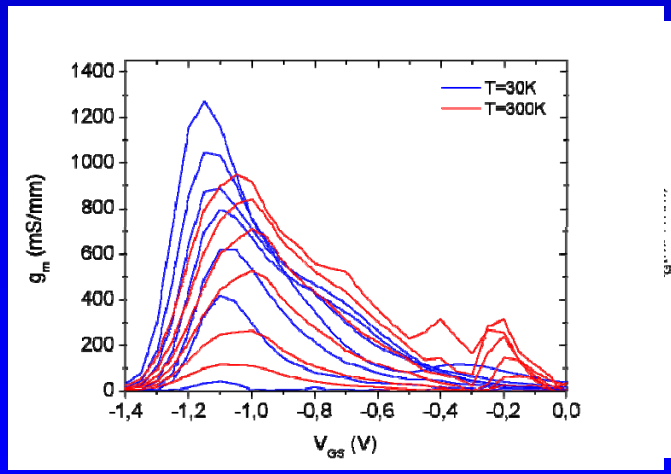
110 nm InAs/AlSb HEMT, 2x50 um

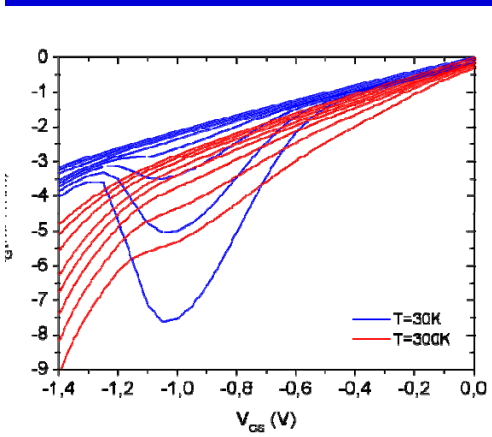
Improvement upon cooling: $R_{on}$ decreased from 0.5 Ωmm to 0.3 Ωmm

The maximum transconductance increased from 950 mS/mm to 1280 mS/mm (VDS=0.5 V)

No observed kink behaviour



# Conclusions

- Establishment of a full wafer process for noise-optimized InP HEMTs for cryo LNAs
- Gain ≈ 39 dB +/-1 dB at optimum bias well in parity with cryo 3 by NGST
- NT < 3K, slightly higher (0.4-0.5K) than cryo 3 by NGST
- At extremly low bias H805, Q4 has better noise performance than cryo 3 by NGST
- A new technology explored: InAs/AlSb HEMT