A complete approach:

From InGaAs channel to cryogenic amplifier

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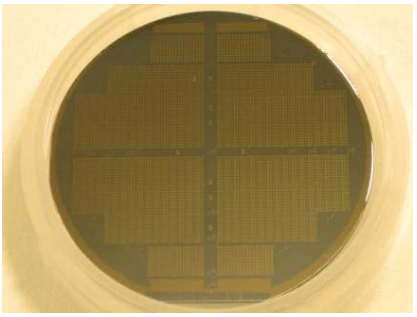
Abstract

The InGaAs-based HEMT (or InP HEMT) is still the best alternative for the first transistor stage in cryogenic LNAs for microwave/mm-wave applications. However, the InP HEMT is not an off-the-shelf component and the relation between device quality and noise performance in the LNA is complex.

In this project, we have established a full-wafer 110 nm InP HEMT process with enhanced reproducibility and stability. This is made within the framework of an ESA-ESOC project for base stations. InP HEMTs are implemented in hybrid IF modules for 4-8 GHz and 32 GHz.

InP HEMT Process

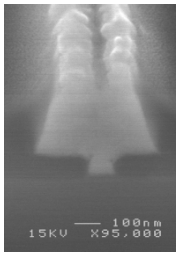
The Nanofabrication Laboratory at Chalmers where the processing was performed.



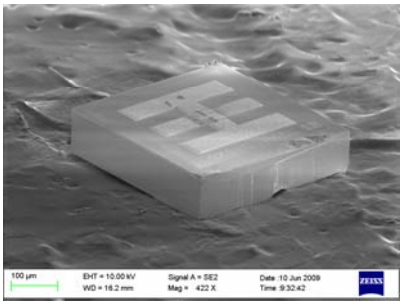
2” InP wafer with 6000 transistors.

Parameter	H805
Yield	> 90%
Fmax/Ft 2*20µm	260/150 GHz
Fmax/Ft 2*50µm	240/240 GHz
Vbgd	8.6 V
Gm_max	1000 mS/mm
Id_max	550 mA/mm
Ig at typical low noise bias	10nA
Rds_on	0.85 ohm*mm
Cgs at low noise bias	575 fF/mm

Transistor data (at room temperature)

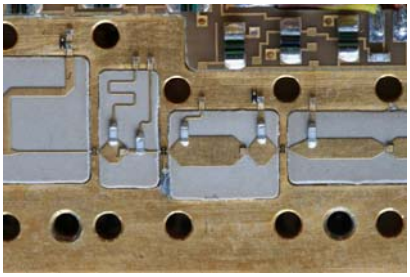


Mushroom gate. The gatelength is 110 nm.

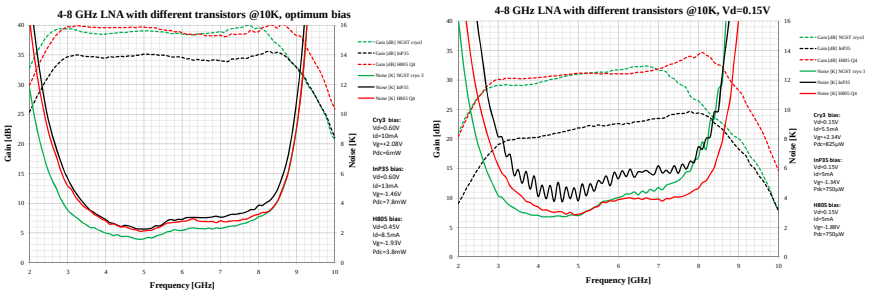


A single InP HEMT, diced from a 2” wafer.

4-8 GHz LNA



4-8 GHz LNA equipped with Chalmers InP transistors



Measured noise and gain of the LNA at 10 K. The results from this work (red) are compared to results with transistors from NGST (green) and earlier Chalmers results (black). To the left are results at optimum bias, and to the right at a very low drain bias of 0.15 V corresponding to a total DC power of consumption of 750µW.

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