12 october 2010

Board Presentation and design (Gijs)
finalized design
production of uniboard
start some testing
some modifications resulted from these tests
DFM ? optimize design for production / fabrication
PCB design : 4 blocks of "2 chips" rotated by 90?
boundary scan test, DDR3, IO interface 6.5Gb/s and 10Gb/s, adc interface up to 200MS/s
some issues discovered (slide 7)
Eye diagram of the optical transmission performed : clean
DDR3 eye diagram is ok
ball soldering problem (DDR3), not seen at Xray inspection, seems to be randomly placed on the board
boundary scan on memory lanes
FPGA have been removed but nothing discovered
no connection between pad and DDR3 interface --> pcb crack in between
only one card produced, problem on this card
no clear explanation up to now, investigation with pcb manufacturer to identify which is the weak point of the design
changes for rev2 of the board already done (slide 14)
meachnical box with optimal cooling, uniboard cards can be stacked
48V fans, works at power on
documentation available on the wiki
final redesign : find cause of the DDR problem, finish testing, etc. (slide 20)
plan for a rev3, astron project considered (apertif) (slide 22)
ADU = adc board

Proto and test at Astron (Heargraves/Kooistra)
test each interface separately
configuration from JTAG or from flash ok
plan to configure from the ethernet to the flash
DDR testing : peuso random patterns for each address --> connection problem discovered
altera IP used for communication with the DDR, works above altera specs
10Gb/s tested : ARP and UDP packet transmitted, rx - tx swap discovered
some errors appear, could be due to non optimal parameters in the tx gain, emphasis, etc. can be tuned on the flight.
tests performed with different link length (1m, 2m, 10m)
tests of the FN - BN mesh : 16h for 8 FPGAs at 6.25Gb/s ok
12 TX tested among 16, but maximum rate achieved ???
BN - BI interface test
BN - ADC interface test with 8 bit 200MS/s counter data
1GbE ok between the 8 nodes, communication between the nodes and RJ45 on going
some tests with i2c interface
watchdog funtion ok
tcl scripts available for compilation, synthesize, ip genration, etc.
implements all these test functionalities into a single design for easy testing of the 8 production uniboard cards.
complete test performed by ASTRON before delevery to other institutes
everything available on the wiki to perform tests by ourselves

Uniboard production and Institutes (Arpad)
video

How to interact with Uniboard (Verkouter)
1Gb/s to NIOS registers to VHDL registers
client running on a control computer to nios CPU via ipv4
client request to the server
UDP/IP packet
uniboard command packet description
read/write/modify N 32 bit words to/from the NIOS
server in C
client library requirements : write to 1 or several FPGAs, safe communication even if a FPGA is broken, etc.
client library : C, C++ or python ?
erlang has been chosen because made for binary data processing and very high level
example of erlang scripts
possibility to interface with python using "port"
it is not planned to transfer data but to configure/monitor FPGA

Modular design and reuse example 1Gbe module VHDL (Kooistra)
why ? for fast designing at the price of much effort at the beggining
from top to bottom : design / module / component
Memory Mapped (bidir data and control) vs streaming (unidir data and bidir control)
MM and ST are Altera terminology for avalon bus
connect VHDL module to NIOS using SOPC and streaming interface
software : *.h (public), ?_regs.h, *.c (private)
module description document with predefined section
module can be made available in Altera SOPC builder

EVN correlator design (Heargaves)

from FN to BN : station data in to 10Gbe ports, correlation products out to backend computer
needs 4GB DDR for FN
128MHz BQ, 2pol, 8 bit *8 station (FN)
BN 2112 corr products 32MHz BW (BN)
proof of concept : 4*16MHz BW per station, 2 pol, 2 bits per sample
then only one FN required, correlation products can be read throug 1Gb/s BN
validity bits are used to tell the correlator which data to process
FN = phase rotator + polyphase filterbank + requantization to 9 bits + framer to mesh
each PFB produces 4096 frequency bin, can clock at over 300MHz but 266.5 chosen = DDS3 local bus speed
= 4 times what is required for 64MHz (complex) but constraints due to memory
BN = DDR3 memory controler and correlator
132 MAC cells clock > 260MHz, 36 bit accumulation
one half DSP block + 72 regs per MAC
cross products, 16 passes ?

Correlator control system (Des Small)
data mostly comes in MarkIv format
correlator based on vdif format
compared to current system :
smaller and simpler
not hard real time but soft real time
erlang

DBBC (Gianni)
general purpose dbbc for radio
4GHz input band = 8GS/s
64MHz/ch output = 128MS/s
each SB independantly tunable
output format : vdif, encapsulated UTP jumbo packet
architecture can be adapted to "any" BW skipping/adding some chips
high sfdr using polyphase filter : 18 bit mult = 85dB, filter design 85dB stopband
VDIF formatter : independent for each dBBC because different IP/port for each dBBC
packet size max 32kbit
function distributed in FN and BN
whole function in FN and BN seen each as a single sopc module
resource usage is low, specially for logic
possibility for larger frame size
possibility to implement RFI within the dBBC
8GHz BW could be tried
possibility to implement FFT part of FX correlator (e.g 4GHz 64kpts)
possibility to implement stand alone spectrometer
1GHz band can move whole design into a single chip
present design assumes 6 bit sample, can be extended with no problem to 8 bits because it is what can handle the input
architecture adequate for interleaved adc
question about the vdif format

RFI mitigation implementation for pulsar radioastronomy
idea is to have basic module that can be added at different steps of the DSP flow
mean estimator which goes bias because of rfi
3 samples 3 sigma detection
30 samples 0.8 sigma detection
radar blanker on real data in real time (on Nancay digital backend)
can be implemented just after digitization or after digital filtering
cyclostationary detector
blind giant pulse detector

RFI mitigation options for Uniboard2 (Weber)
possibility of implementation in the dBBC
for uniboard 2, possibility to implement RFI mitigation in the beamformer and in the correlator (rfi mitigation, spatial filtering, estimation & substraction)
cyclic spatial filtering

Application at Korean Institute (Sohn/Jung)
Korean VLBI Network = 3 antennas
part of East Asian VLBI Network
KVN data acquisition system : Antenna site / Main site = digital filter + digital correlation (presently)
for next generation : uniboard could be used for main site to process data before correlation
3 cards required at least to process each station flow

Multi Uniboard application example of the apertif beamformer (Kooistra)
architecture uses independency of
subbands (different freqs)
beams (different directions)
multi-uniboard system connecting via swich network
multi-uniboard system via backplane
using this scheme = possibility to connect between FN (or BN)
APERTIF beamformer for Westerbork Radio telescope

APERTIF = 96 Uniboards, 192 ADC United, 24 Uniboard for correlation

ADC & Uniboard in Nan?ay
6 bit ADC @ 3GS/s bipolar technology 0.25um
scrambler function available (in the chip ?) to enable clock recovery from the FPGA RX
two test benches : 1 uses GbE (validated up to 2.8GS/s), 1 uses demux output
Uniboard and digital front-end : flexible 10GbE interface to transfer data from the antenna to the Uniboard
FMC interface (HPC connector), pinout is normalized
national funding requested, if funded, the pcb layout will be available to the Uniboard members

13 october

Shanga?
new correlator for chinese VLBI network
2-4GHz per station, 16 ? stations
8 receivers for new 65m telescope
DBBC 4 IFs 2-4GHz, 32 subchannels SBW = 64MHz 1, 2 ,4 or 8 bits
spectroscopy : 50Hz in 32MHz BW
7 beams on telescope, beam former is required
digital backend descoped version 2012, final version 2-4GHz 2015
2012 correlator working
questions from shanga? : status of Uniboard 1, possibility to purchase large number of uniboard, possibility to share IP ?
end of 2011 : call for uniboard card institute need (including lofar, chinese, etc.)

FP7 (Arpad)
AArTFACT, APERTIF
uniboard2 possible JRA in radionet3
~same participants
HW, FW, SW design as uniboard 1
particular attention to power efficiency
production ready 2015-2016
design based on 28nm or beyond generation
40G/100G
hardcopy, partial hardcopy
strict desing reuse policy
altera university program : ip could be cheaper