Fast ADCs and Uniboard
Overview and road map at LAB/UB

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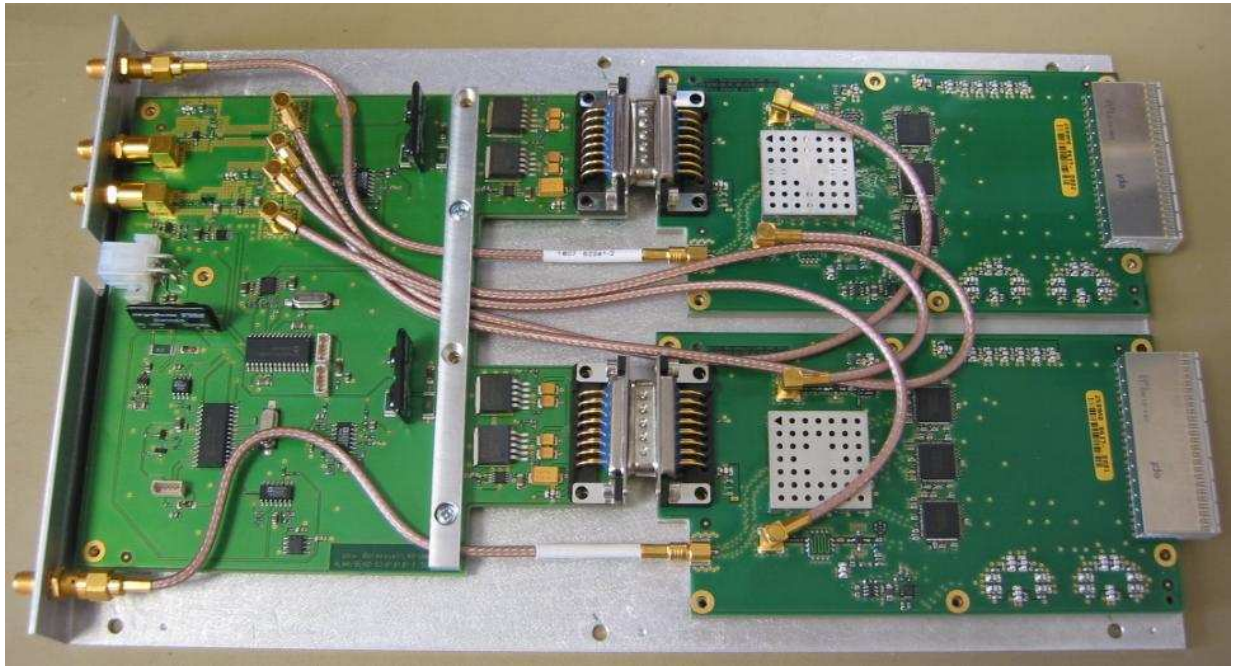
Plan

- Historical Background
- Current Designs
  - Digitizer Module based on commercial components
  - ASIC design
- Connecting to the Uniboard
- Future Designs (and Uniboard2 ?)

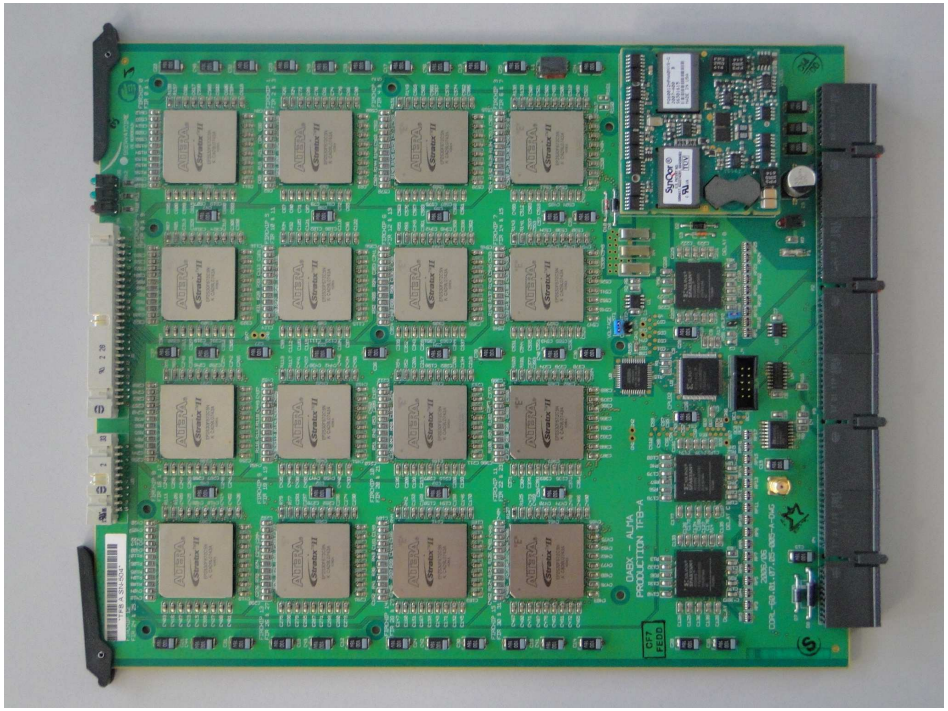
Historical Background

- LAB / UB1 designed several generations of digitizers and demultiplexers for ALMA
  - ALMA digitizer : 3bits, 4GS/s, 2-4GHz BW
  - ALMA demultiplexer : 1:16 4GHz



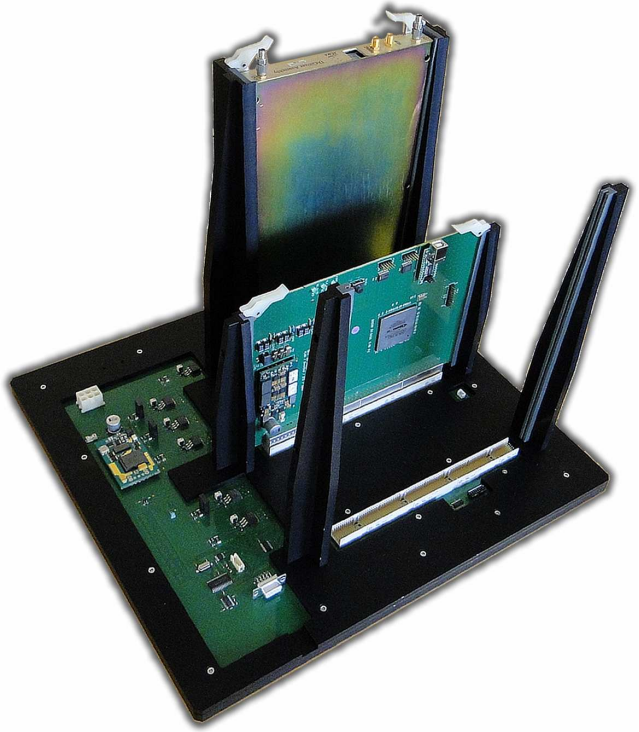
Historical Background

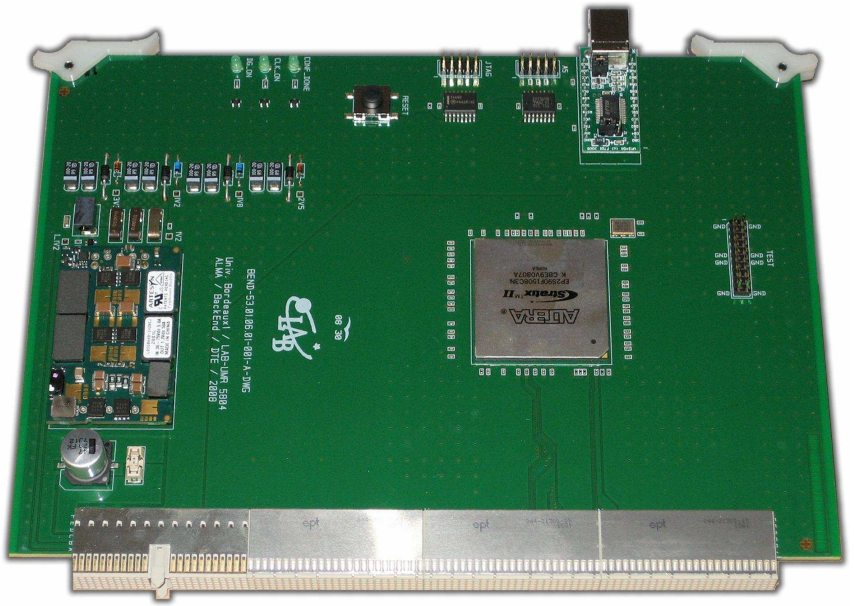
- LAB / Arcetri designed the digital filter bank of the ALMA correlator
  - tunable filter 2GHz input for 62.5MHz or 31.25MHz output
  - 32 filters per 2GHz baseband = one board



Historical Background

- LAB designed the Digital Test Equipment for the ALMA DiGitizer module





Current Designs

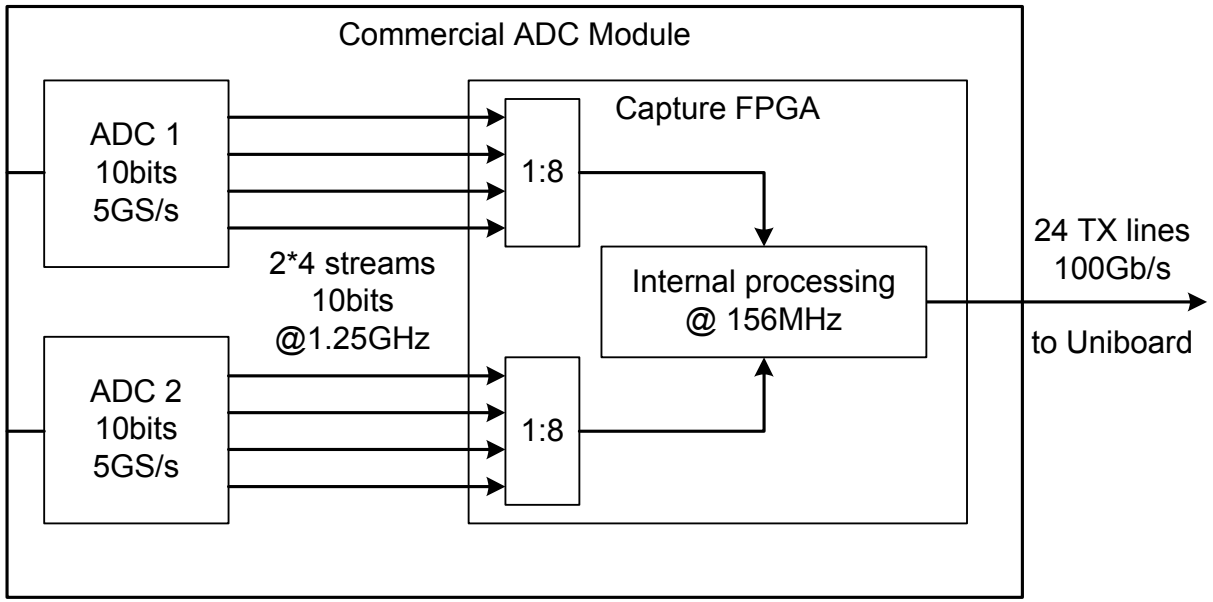
- Design of fast digitizer modules with on the shelf components
  - First generation : 2* 10bits, 5GS/s, 3GHz
  - Second generation : 10 bits, 10GS/s, 3GHz

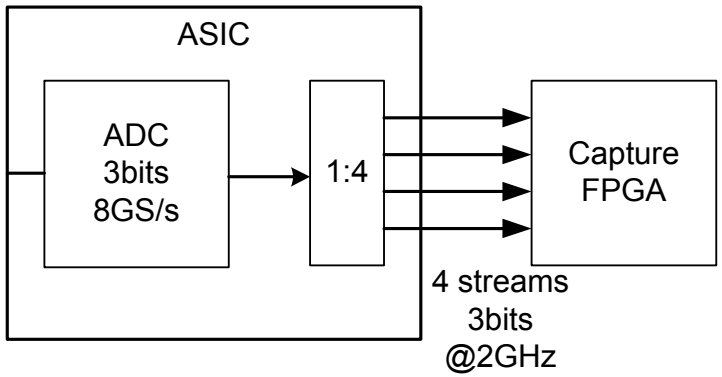
- Collaboration with UB1 to design new ASICs
  - ST microelectronics technology : CMOS 65nm
  - T&H module : 5.8 ENOB , 8GS/s, BW -3dB 8GHz
  - Next chip : 3bits, 8GS/s, BW -3dB 8GHz, DMX 1:4

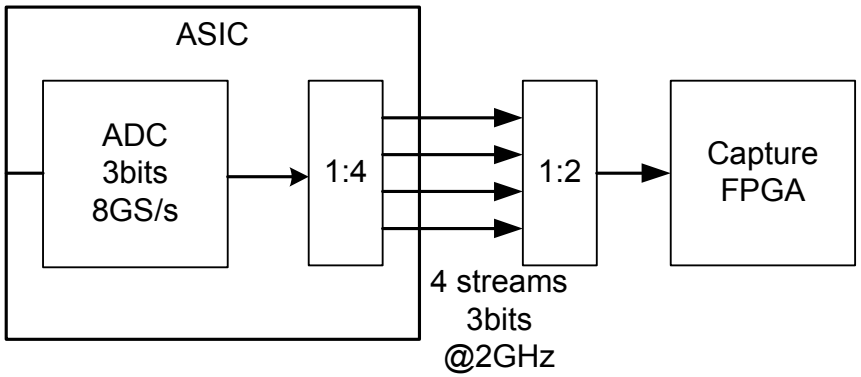
Connecting to the Uniboard

- Strategy :
  - minimum demultiplexing stage by full custom design or commercial chip
  - FPGA module responsible for capturing data from demux and feed the digital processing stage (e.g. Uniboard)
- Which logic standard, protocol ? Parrallel bus, Altera Serial Lite, Ethernet
  - No protocol between ADC and capture FPGA, 1.6Gb/s
  - High speed serial link between capture FPGA and DSP
- Uniboard Specs :
  - 4*32 parallel links @ 1.6Gb/s
  - 4*16 RX lines @ 6.375Gb/s
  - Gb Ethernet : 16 @ 10.325Gb/s

Connecting to the Uniboard







Road Map

- End of 2010 : run for ASIC ADC 3 bits, 8GS/s + DMX
- Q1 2011 : test with 1st « commercial » prototype 10 bits 5Gs/s
- Q2 2011 : test with ASIC module
- End of 2011 : run for new T&H
- Q1 2012 : test with 2nd « commercial » prototype 10 bits, 10GS/s
- End of 2012 : run for new ADC (6 bits, 8Gs/s)