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Netherlands Institute for Radio Astronomy

The UniBoard: a Multi Purpose FPGA Rich Board

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Introduction ASTRON

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Institute in Dwingeloo

Radiotelescope in Westerbork


jive
JOINT INSTITUTE FOR VLBI IN EUROPE
(c) E.P.B. 2006

ASTRON's radio telescopes

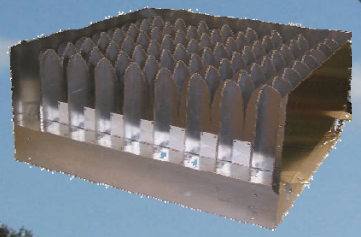
LOFAR core near Exloo

Westerbork

Dwingeloo

Saturday 12 June 2010: LOFAR Opening

APERTIF



Square Kilometer Array (SKA)

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RadioNet FP7

- European program for radio astronomy with 26 partners
- Several joint Research Activities one of which is UniBoard

Contract no. 227290

Why UniBoard?

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- Increase processing density to be ready for the peta Flop era
- Serve new (short term) applications
- Pave the way to the SKA
- “Generic” hardware architecture tailored to …

Targeted Applications

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- APERTIF Beamformer (Astron)
- APERTIF Correlator (Astron)
- EVN Correlator (JIVE)
- Digital Receiver (Observatoire de Bordeaux, Instituto Nazionale di Astrofisica)
- Pulsar Binning Machine (Manchester Univ., University d'Orleans)
- All dipoles LOFAR Station Correlator (University of Oxford, Astron)

UniBoard Philosophy

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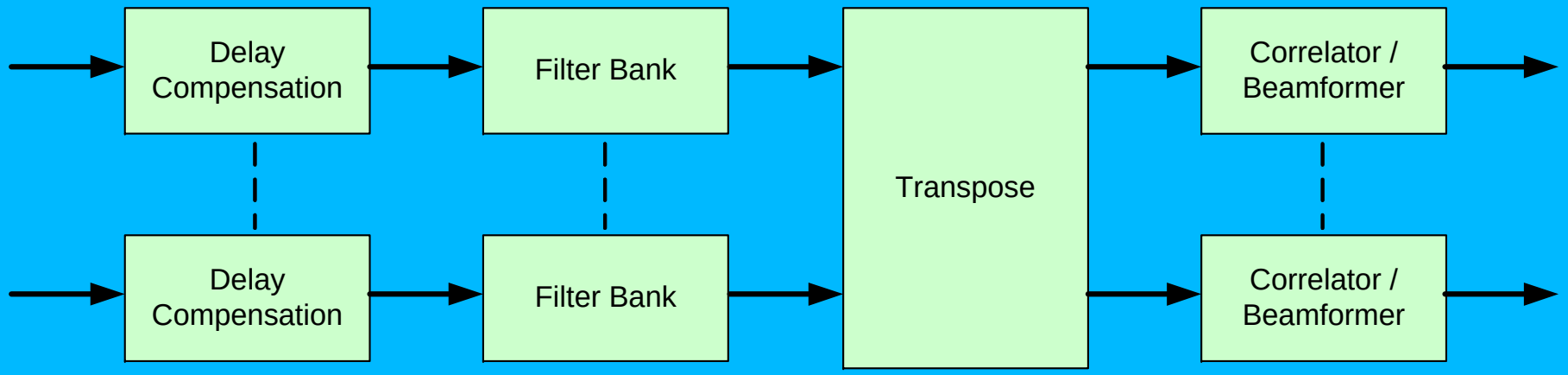
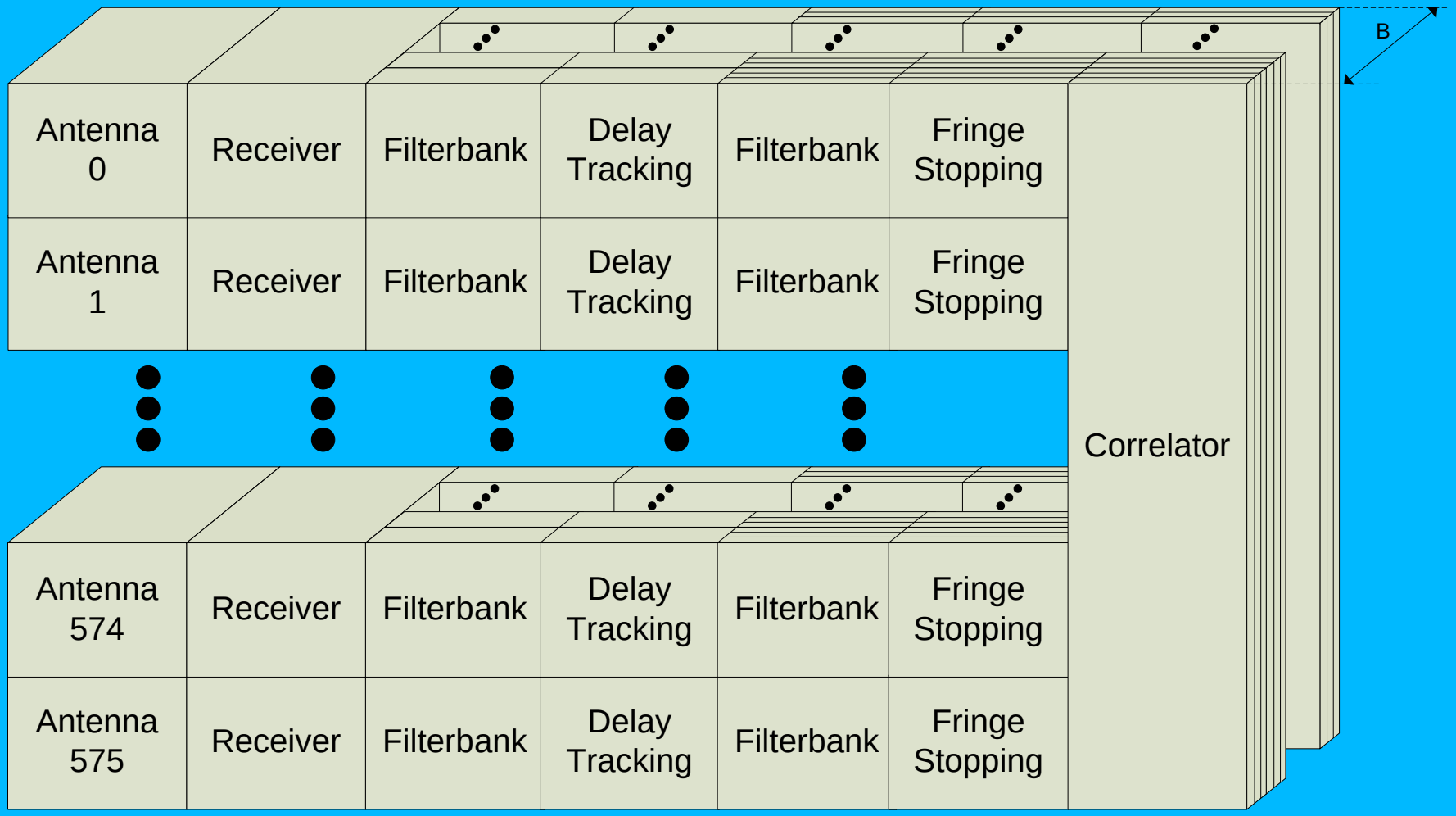
- Continue on the approach we had for LOFAR:
  - High integration density
  - Scalable allowing one, more or many boards
- Use 10GbE interfaces for data IO
- All FPGAs should have the same capabilities
- Usage of one type of board for multiple applications
- The firmware makes the board application specific

Typical Signal Processing Flow



Typical FX Correlator Architecture



Types of Processing Targeted for UniBoard

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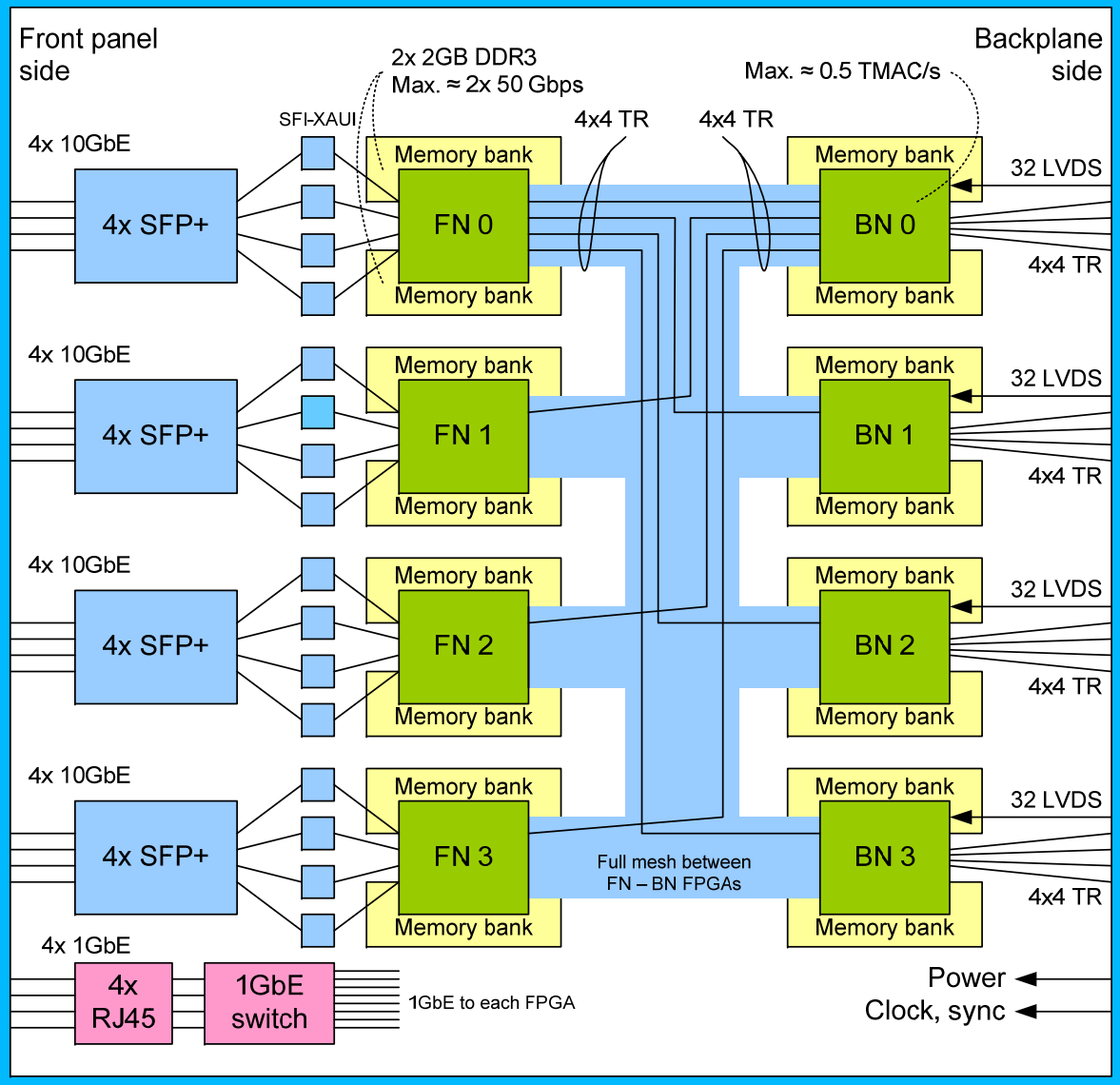
- Input processing
  - Filterbank
  - Digital receiver
- Output processing
  - Beamformer
  - Correlator (FX)
  - Pulsar processing
- Architecture uses the independency of:
  - Subbands (different frequencies)
  - Beams (different directions)

UniBoard Block Diagram



UniBoard Layout

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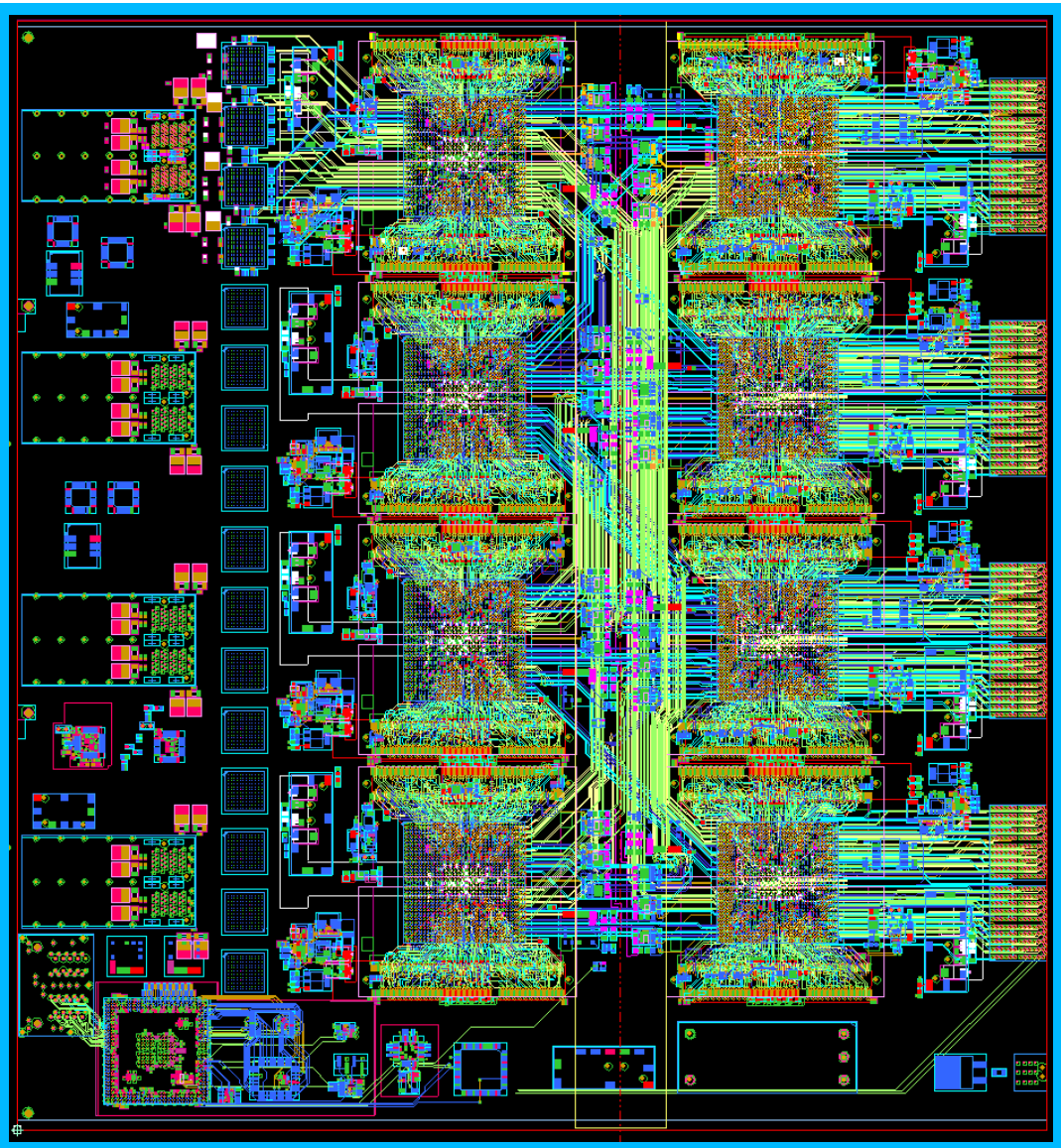

- H x D x T = 9HE x 340 x 2.4mm
- 14 layers PCB

UniBoard Prototype

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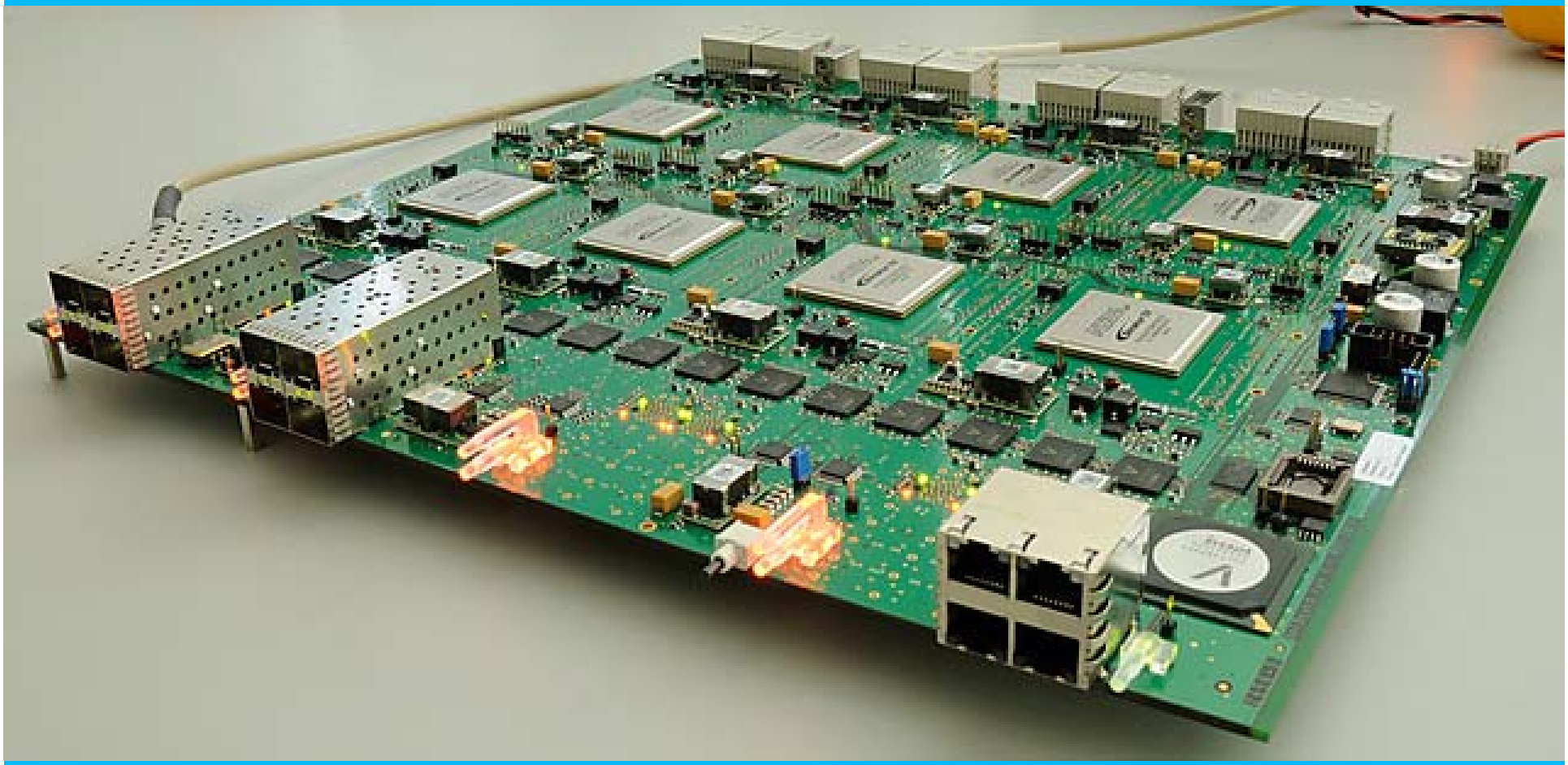

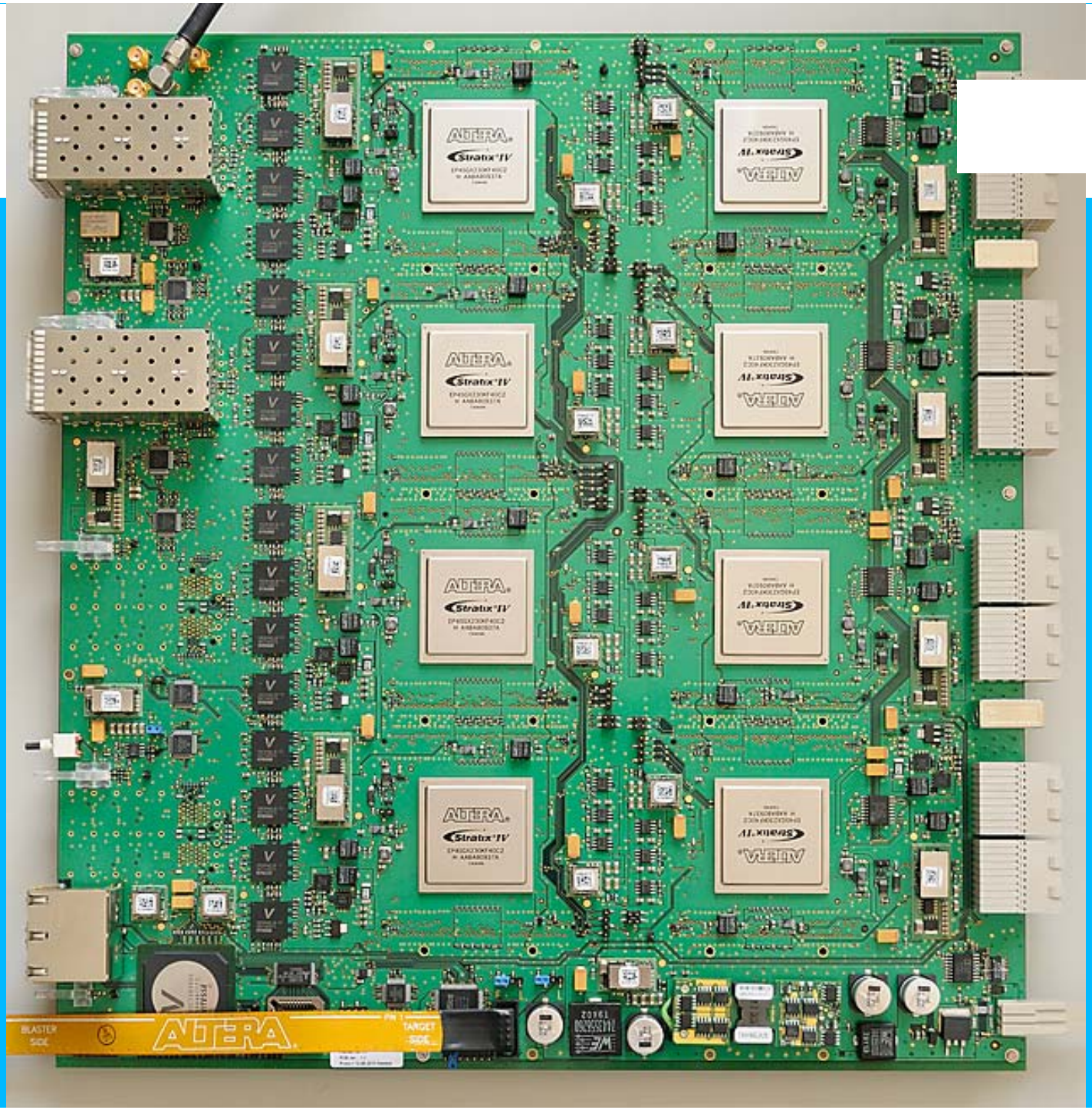
ALTERA
Stratix IV
BLASTER SIDE
TARGET SIDE

Extending Uniboard to a System

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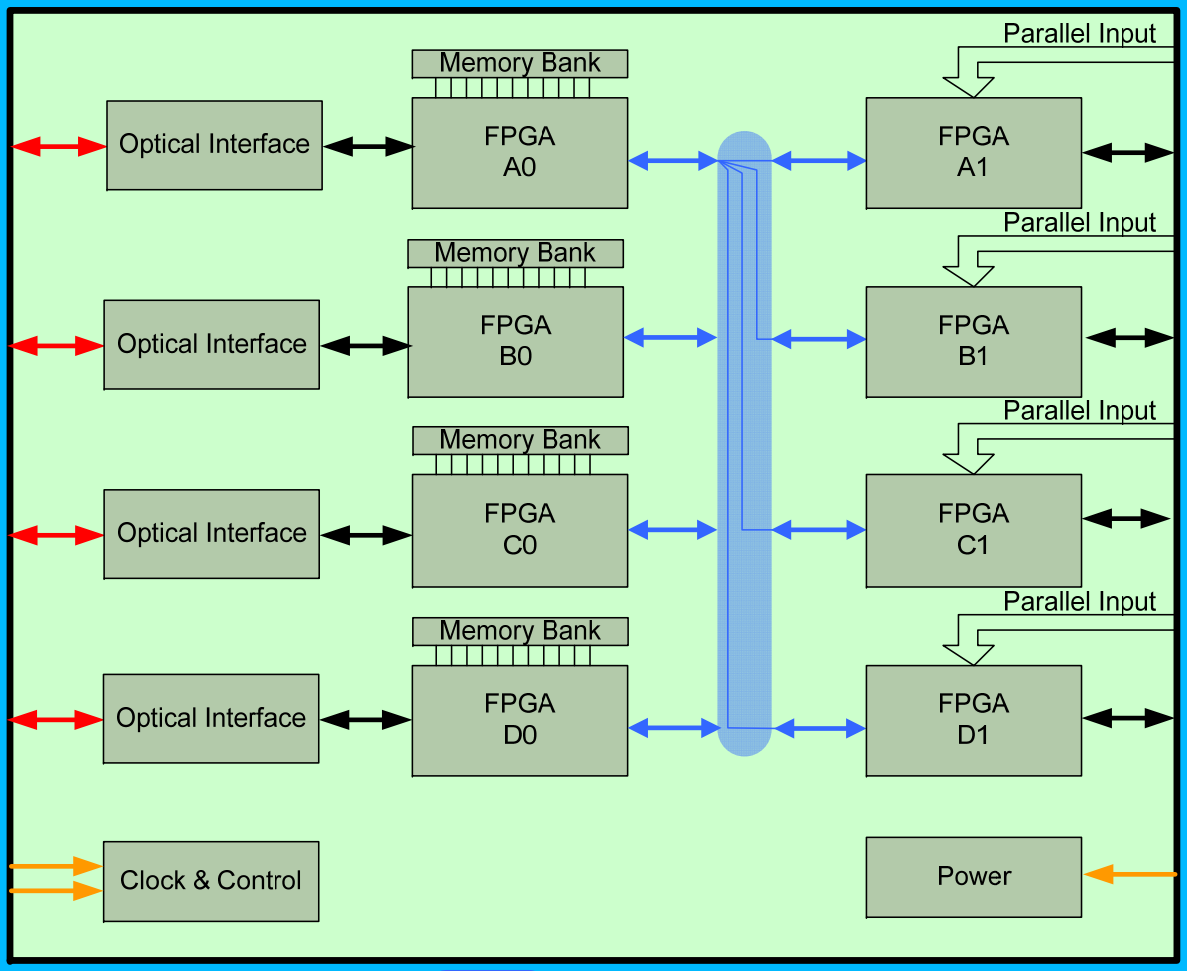
- With N nodes each node processes 1/N part of the total processing
- Board level:
  - each input node communicates to all output nodes
  - each output node communicates to all input nodes
- System level:
  - each output node communicates to the same output node of each board (all A1's, B1's, C1's and D1's)


Parallel Input
Memory Bank
Optical Interface
FPGA
A0
FPGA
A1
Parallel Input
Memory Bank
Optical Interface
FPGA
B0
FPGA
B1
Parallel Input
Memory Bank
Optical Interface
FPGA
C0
FPGA
C1
Parallel Input
Memory Bank
Optical Interface
FPGA
D0
FPGA
D1
Clock & Control
Power
Mesh between all input and all output fpga's
multi x Gb Transeiver fpga-to-fpga connection
Multi Gb Transeivers or 10GbE board-to-board connections
multi x 10GbE IO connection

APERTIF Requirements

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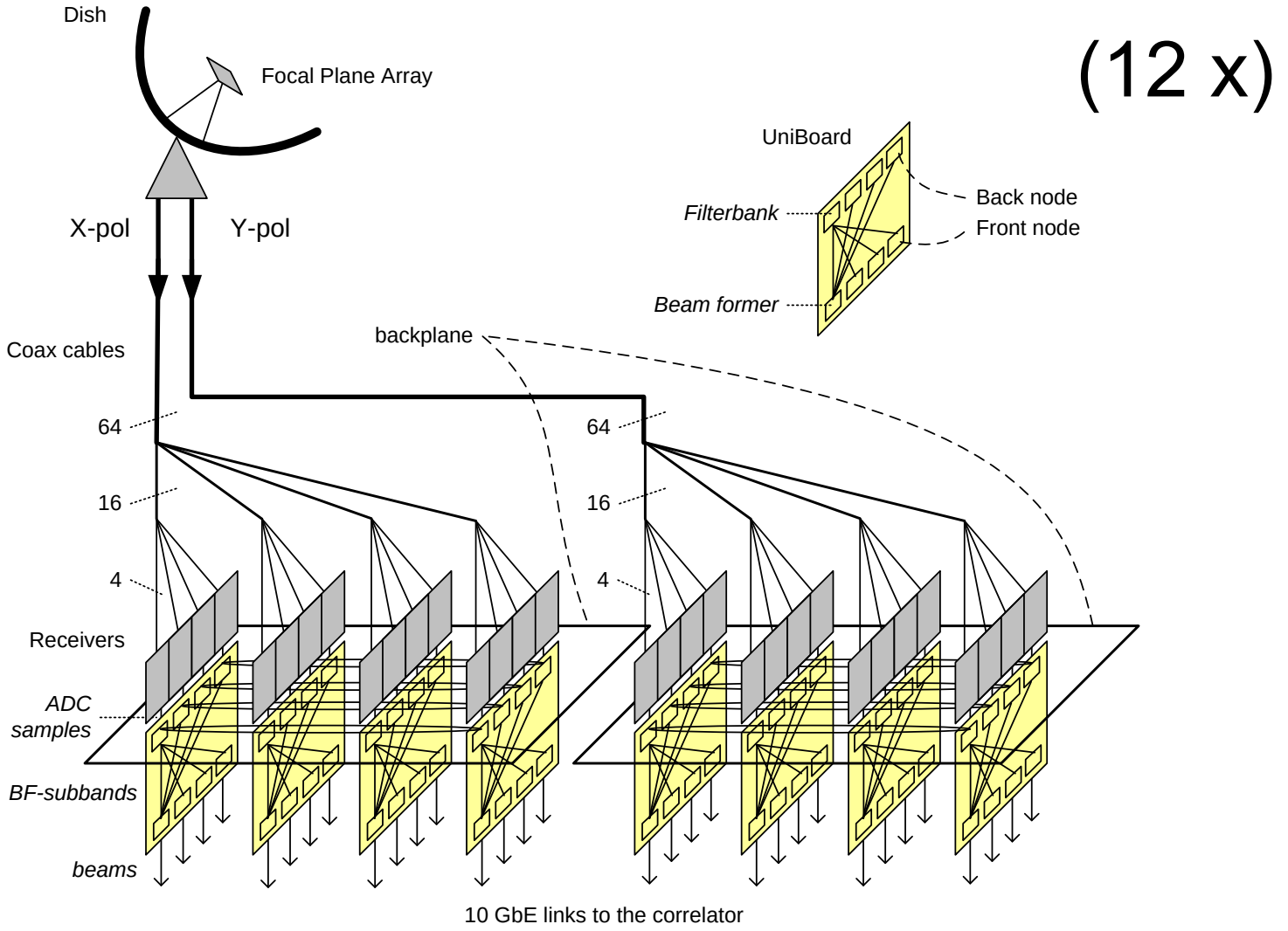
- Beam former:
  - 12 Westerbork 25 m dishes each with a Focal Plane Array
  - 60 dual polarization antennas per telescope
  - 400 MHz RF input bandwidth
  - 300 MHz beam output bandwidth
  - 37 beams

- Correlator:
  - 12 dual polarization FPA telescopes
  - 37 beams, so in total 11000 visibilities

UniBoard for APERTIF Beamformer



UniBoard for APERTIF Correlator

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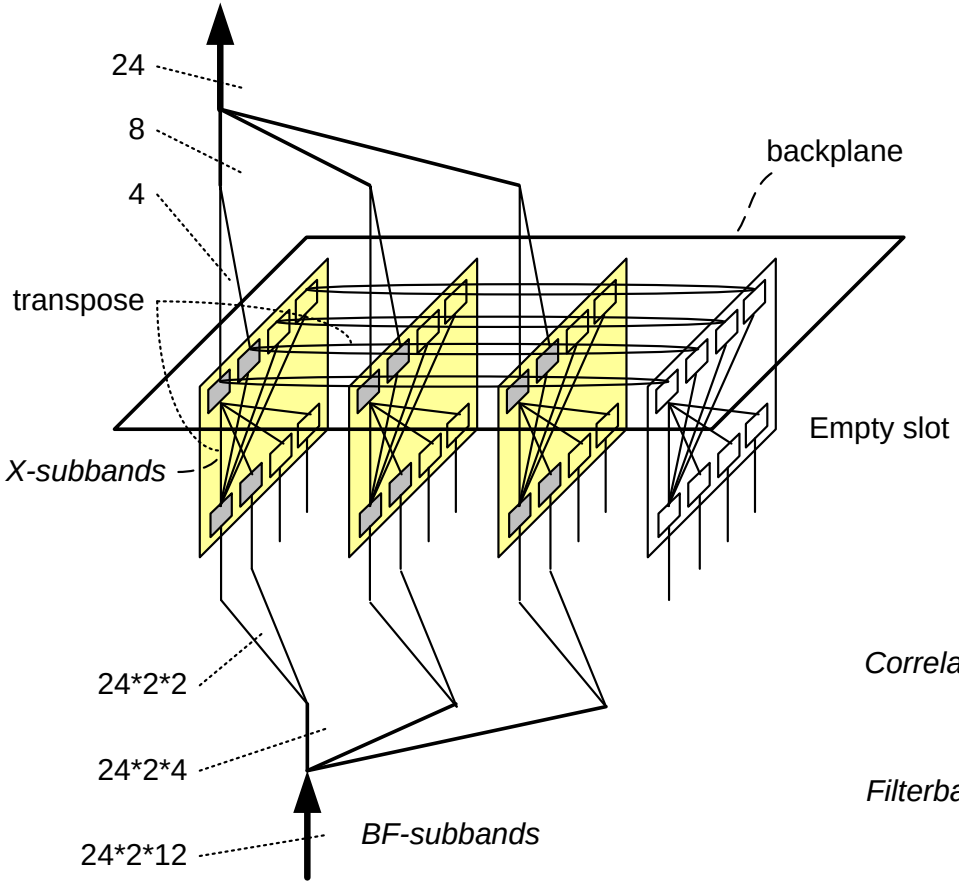
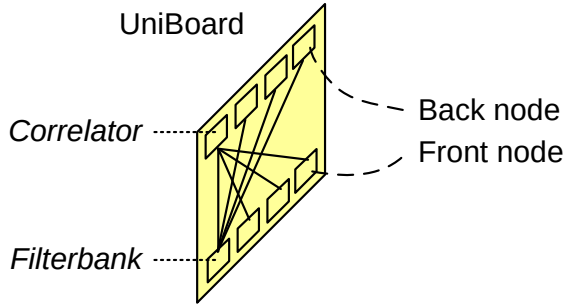
Full Stokes visibilities of 24 BF-subbands bandwidth and for all beams to the post processing via 1 GbE control links



(8 x)



All beams with each 24 dual pol BF-subbands from 12 telescopes

UniBoard for APERTIF Summary

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Processing	Processing [TMAC/s]	Nof UniBoards (FPGAs)	Utilization GMAC/s/FPGA
APERTIF BF	94	96 (768)	122 (24%)
APERTIF X	25	24 (192)	130 (25%)

IO	Data rate [Tbps]	Nof 10GbE (front FPGAs)	Utilization Gbps
APERTIF BF	Out: 2.1	384 (384)	5.5 (55%)
APERTIF X	In: 2.1	384 (96)	5.5 (55%)

UniBoard Conclusion

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- Integrated solution using
  - multiple FPGAs per board
  - multiple boards in a subrack (continue on LOFAR experience)
- Per UniBoard 4 front node FPGAs and 4 back node FPGAs:
  - 8 x two DDR3 memory banks
  - 4 x four 10GbE links at the front
  - 4 x 16 transceiver links at the back
  - 4 x 32 bit LVDS inputs at the back to connect ADCs
- One type of board suitable for many applications