ASTRON
Netherlands Institute for Radio Astronomy

UniBoard2 Manual

	Organisatie / Organization	Datum / Date
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1 Introduction

Please read the following manual carefully before using your UniBoard^2. This manual contains important information on how to properly operate this unit. In this manual the safety and regulatory information is included. In this manual the parts included in the delivery package as well as peripheral parts for UniBoard^2 are described. In a separate section optional parts are discussed.

All boards are tested with boundary scan and functional tests using the peripherals as described in this document.

1.1 Reference documents (RD)

Reference document which can be found on http://www.radionet-eu.org/radionet3wiki/doku.php?id=jra:uniboard2:documents (ask for more details about the wiki Arpad Szomoru, szomoru@jive.eu)

Ref.nr.	Document number	Title
RD-1	ASTRON-RP-1519	Risk analysis report UniBoard2
RD-2	ASTRON-RP-1520	Measurements for CE

2 Safety, Regulatory and Environmental Information

2.1 General Safety Considerations

WARNING	If this product is not used as specified, the protection provided by the equipment could be impaired. This product must be used in a normal condition (in which all means for protection are intact) only**.**
CAUTION	Ventilation Requirements: When installing the product in a cabinet, the convection into and out of the product must not be restricted. The ambient temperature (outside the cabinet) must be less than the maximum operating temperature of the instrument by 4 °C for every 100 watts dissipated in the cabinet. If the total power dissipated in the cabinet is greater than 800 watts, then forced convection must be used.
WARNING	These servicing instructions are for use by qualified personnel only. To avoid electrical shock, do not perform any servicing unless you are qualified to do so.
WARNING	The opening of covers or removal of parts may expose dangerous voltages. Disconnect the UniBoard^2 from all voltage sources before it is being opened.
WARNING	UniBoard^2 is made for indoor use, don't expose the device to water.
CAUTION	The customer has to include over temperature protection in the firmware.
CAUTION	Changes or modifications not expressly approved by ASTRON, which is responsible for CE compliance, could void the user's authority to operate this equipment.

2.2 Preventing electrostatic discharge damage

Protection against electrostatic discharge (ESD) is essential while connecting cables and assemblies (DUT) to the UniBoard^2. Static electricity can build up on your body and can easily damage sensitive internal circuit elements when discharged. Static discharges too small to be felt can cause permanent damage. To prevent damage to the UniBoard^2:

- always have a grounded, conductive table mat in front of UniBoard^2.
- always wear a grounded wrist strap, connected to a grounded conductive table mat, having a 1 MΩ resistor in series with it, when handling components and assemblies or when making connections.
- always wear a heel strap or ESD shoes when working in an area with a conductive floor. If you are uncertain about the conductivity of your floor, wear a heel strap.
- always ground yourself before you clean, inspect, or make a connection.

2.3 Preventing connector damage

Visual Inspection and Gagging Connectors	
Do	Do Not
Inspect connectors with magnifying glass	Use a connector with a bent or broken center conductor
Look for metal debris, deep scratches or dents	Use a connector with deformed threads
Inspect and gage connectors	Use a connect or with a protruding center conductor
Use correct torque wrench	Use an out-of-specification connector
Making Connections	
Align connectors first	Cross-thread the connection
For SMA connector rotate only the connector nut	Twist connector body to make the connection
Use correct torque wrench	Mate different connector types
Switch off lasers/transceivers on both sides of the cable before changing cables	Look into optical cables and transceivers

2.4 Shipment for service

Contact ASTRON for instructions on how to ship the UniBoard^2 for service. Ship UniBoard^2 only using the original packaging material. Shipping UniBoard^2 in anything other than the original packaging may result in non-warranted damage.

2.5 Regulatory information

This product has been designed and tested in accordance with accepted industry standards, and has been supplied in a safe condition. The documentation contains information and warnings that must be followed by the user to ensure safe operation and to maintain the product in a safe condition.

2.6 CE directive

This product complies with the CE directive (RD-1 and RD-2).

2.7 Waste electrical and electronic equipment (WEEE) directive

Directive 2002/96/EC of the European Parliament and of the Council. The wheelie bin symbol (left) is shown on this product. It indicates that the product should not be disposed of with regular household waste, but should be disposed of separately. Electrical and electronic equipment can contain materials that are hazardous to the environment and human health and therefore should be disposed of at a designated waste facility or returned to ASTRON for the appropriate recycling to take place. If you wish to dispose of this product and the product still functions, please consider recycling/reusing it.

This product has been designed for proto type purposes. Therefor this product is not RoHS compliant. To ensure compliance with the requirement of the WEEE directive, UniBoard^{2}s which achieved at the end of their life must be returned to ASTRON. ASTRON will ensure environment friendly recycling of UniBoard^2.

2.7.1 Known Hazardous materials:

For the production of this board, leaded solder is used.

2.8 Environmental conditions

Uniboard^2 is developed for stationary, 19” rack mount use in a building.
Temperature range: +10C to +30°C
Humidity 20% RH to 90% RH (non condensing)

Uniboard^2 should not be subjected to water.

2.9 Contact information

All inquiries, comments or suggestions concerning this and other ASTRON equipment and manuals should be directed to:

ASTRON
Gijs Schoonderbeek
Oude Hoogeveensedijk 4
7991 PD Dwingeloo
Tel: +31 (0)521-595101

3 Included in the package

Table 1 Package content

	Number	Manufacturer.	Type
UniBoard^2	1	ASTRON	rev 2.0
UNB2_TB_220	1	ASTRON	rev 2A
Memory	8	Micron	MTA18ASF1G72HZ-2G1A1
Fans for cooling	2	ebmpapst	8318 48V DE 63mA 3W
Power connector + cable	1	ERNI	134.464 (D-Sub 3W3 40A)
Heat Exchanger	1	Switftech	MCR-X20 Drive R3
Cooling Liquid	1L	Aqua Tuning	AT-Protect UV-Crystal blue
Fans for Heat Exchanger	2	Swifttech	Helix-120
Metal Housing	1	APRA	CA-423
Optical Cable Assembly	2	AVAGO	AFBR-7QER01Z

4 Peripherals

4.1 Needed peripherals, with recommendations

Table 2 Recommended peripherals

	Specification	Manufacturer	Type
Power Source	48V 500W	Meanwell	RCP-1K1UI-48
JTAG programmer		Altera	USB Blaster2

4.2 Optional peripherals

4.2.1 QSFP+

For the optical interface, QSFP+ cages are placed on UniBoard^2. In each cage a transceiver module or an Active Optical Cable assembly can be plugged. Each FPGA has 6 cages given 24 cages for a single UniBoard^2.

Table 3 QSFP examples

	Specification	Manufacturer	Type
Transceiver	QSFP+, 40Gb, 850nm	Avago	AFBR-79EIPZ
AOC	40GbE, 10m	TE	2123909-4
AOC	40GbE, 1m	Avago	AFBR-7QER01Z

5 Specifications

Table 4 UniBoard² Specifications

Input power	48V DC
Power consumption	450W
Size	435 x 520 x 86.3mm
Weight	9.9 kg
Ambient temperature	10-27°C

6 Switching UniBoard² ON and OFF

The following steps should be taken to switch UniBoard² on:

1. Check Liquid is filled and connected to UniBoard² (see section 12).
2. Switch on pump of liquid cooling.
3. Check ON/OFF switch on UniBoard2 is in OFF mode (see Figure 1).
4. Connect 48V to UniBoard² (see section 7).
5. Connect Optical and other cables to UniBoard²
6. Switch on 48V power supply, the LED in the ON/OFF switch of UniBoard² should be red.
7. Use the switch on UniBoard² to switch on the UniBoard², the LED in the switch should be green.
8. After the FPGAs are configured the LED should be flashing red.

The following steps should be taken to switch off UniBoard²:

1. Use the ON/OFF switch on UniBoard² to switch off UniBoard².
2. When needed unplug optical and other cables.
3. Switch off the 48V power supply.
4. Switch off the pump for the cooling.

In case of power drop a hold-up circuit is placed on UniBoard² to enable power down sequencing of the FPGAs. This function is limited and should therefore only be used in emergencies.

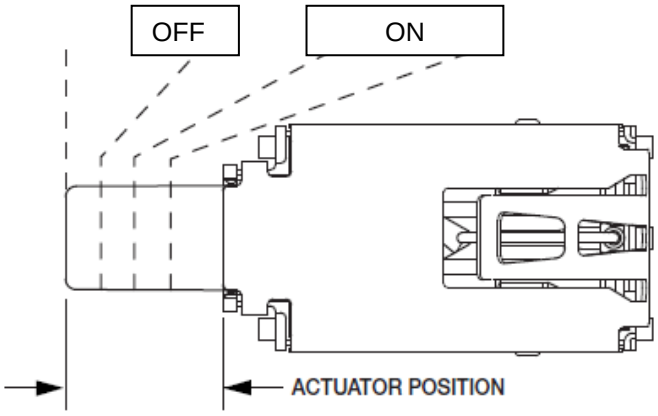

Figure 1 ON/OFF switch

7 How to connect to UniBoard²

In Figure 3 and Figure 2 the front and back side of the UniBoard² housing are shown. In these figures the location of the connections show. Table 5 has a short description of the connections is given.

Table 5 UniBoard² connectors

Connection	Side	Specification
Power	Back side	Isolated 48V DC
Clock	Back side	200MHz
JTAG	Back side	Altera pinning
Liquid cooling (2x)	Back side	QD3 Quick Release
Ethernet	Front side	Standard RJ45
10GbE interfaces	Front side	QSFP+

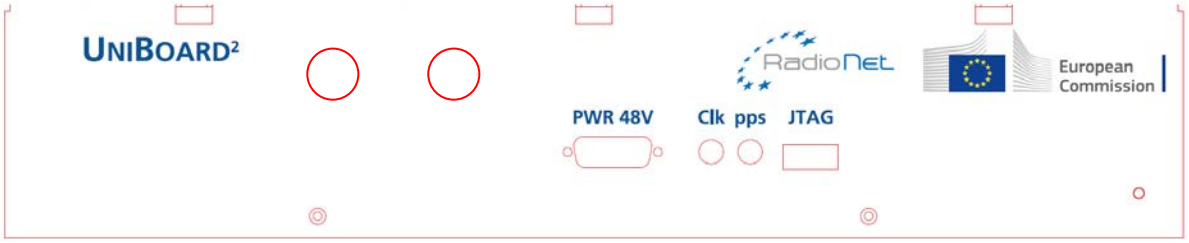

Figure 2 Back side UniBoard²

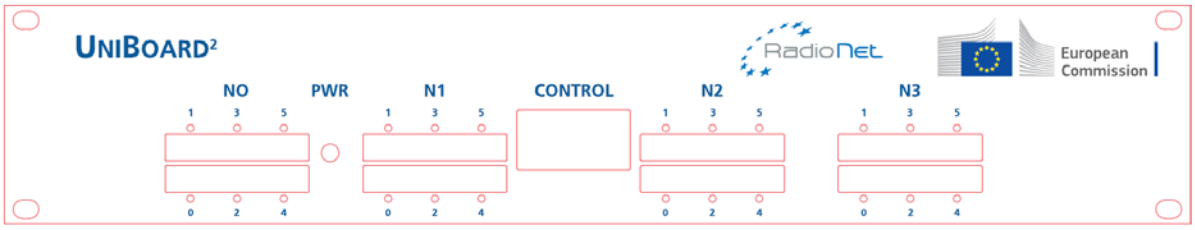

Figure 3 Front side UniBoard²

7.1 Power entry

In Figure 4 an overview of UNB2_TB_220 is given. In this picture the power entry connector is shown.

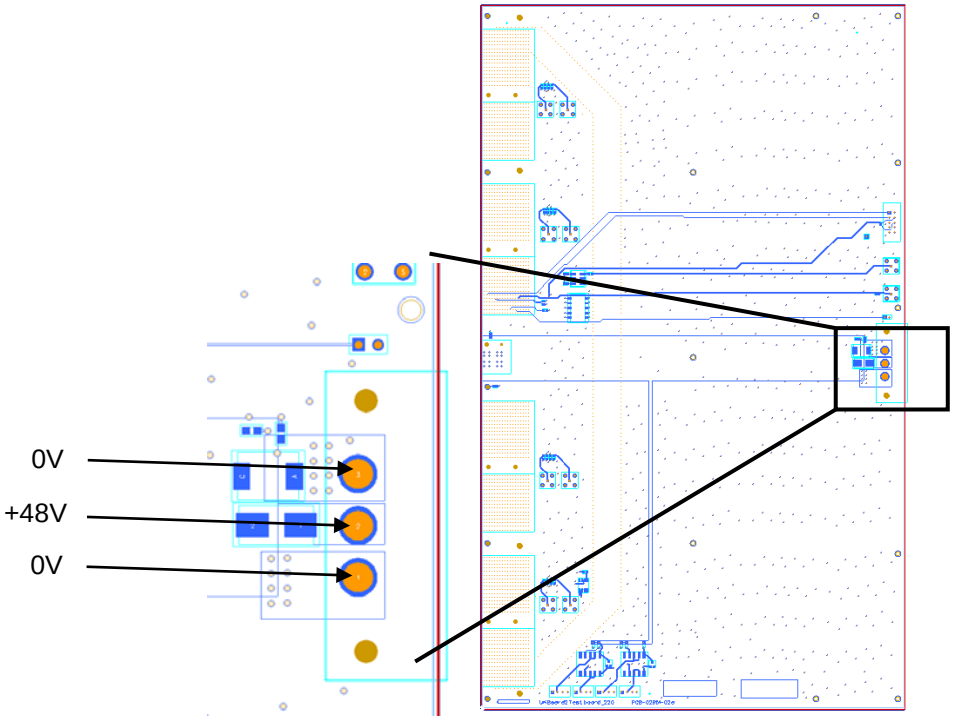

Figure 4 48V Power Entry

48V input remark: UniBoard^2 has an isolated 48V power input. This means that a positive 48V power supply should be connected with the +48V-connection to the pin in the middle of connector P5 and the GND-connection to the left and right pins of P5. Always connect one side of the 48V Power supply to system ground.

7.2 Ethernet control

Up to six Ethernet control cables can be connected to UniBoard^2. Standard CAT6 10/100/1000BASE-T cables can be used. The Ethernet connector is shown in Figure 5.

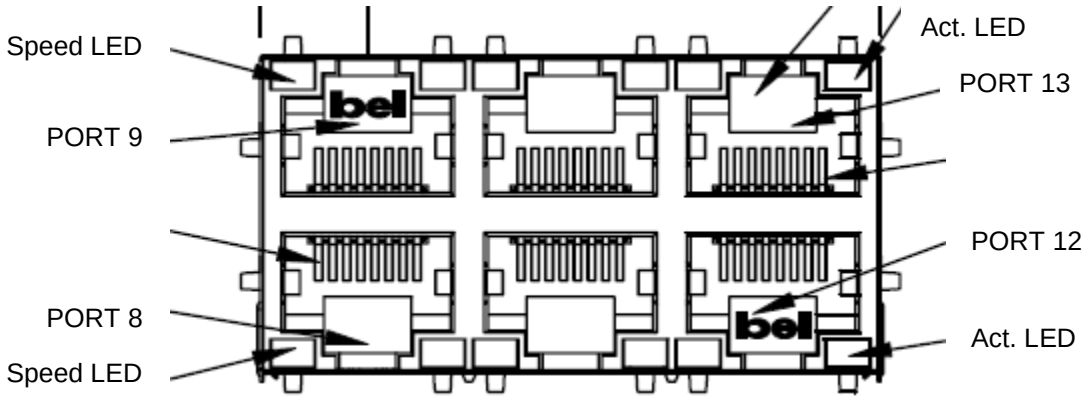

Figure 5 Ethernet Connections

In table the function of the ports are shown. Default all ports are placed in a single VLAN. When needed a different program can be programmed to divide ports over VLANs.

Table 6 Function of Ethernet ports

PORT	Function	PORT	Function
8	VLAN 0	11	VLAN 0
9	VLAN 0	12	VLAN 0
10	VLAN 0	13	VLAN 0

7.3 CLK and PPS-input

The location of the CLK and PPS inputs are shown in Figure 6. Depending on the jumper setting of UniBoard^2 an external clock can be connected to UniBoard^2. This clock can be AC-coupled. The amplitude range should be 0.5-1.5Vpeak-peak, the frequency is dependent on the firmware image. For the pulse per second input (PPS) a DC coupled pulse with a low level between -0.1V and 0.8V and a high level between 2.0V and 3.1V should be used. The length of the pulse is depended on the firmware, in most cases a pulse of >20ns is working. For the PPS a simple pulse generator like the Agilent 33250A can be used. The setting depends on the firmware image. For the test image a pulse with an edge time of 5ns, a pulse width of 5ms and a period of 1s can be used. This pulse generator can be locked to the clock through the 10MHz reference input.

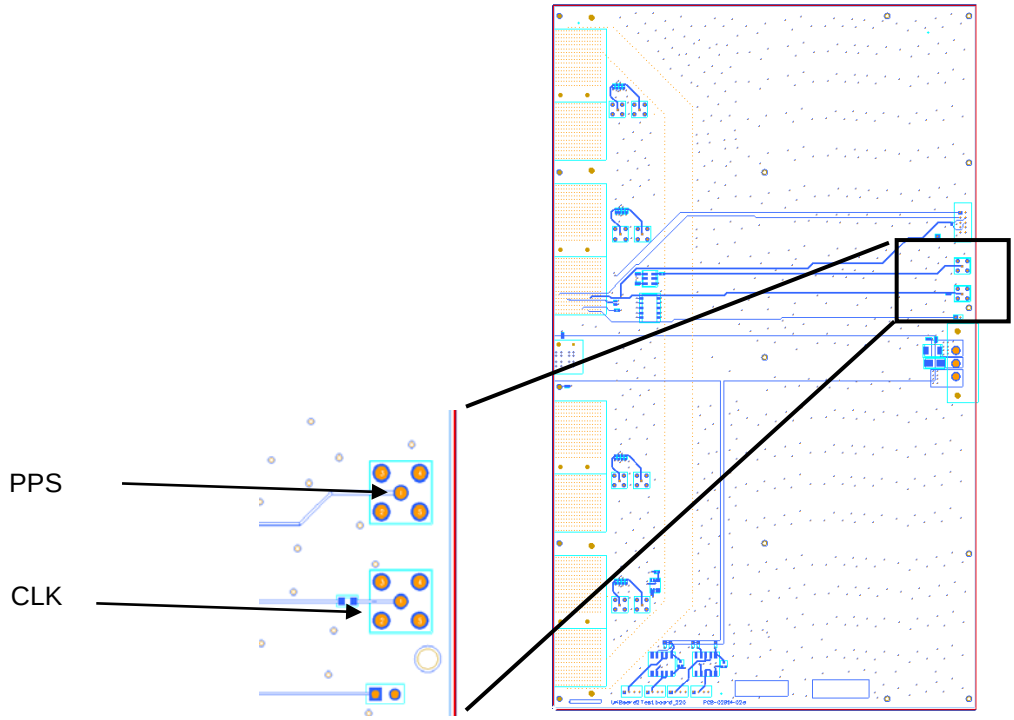

Figure 6 Location of PPS and CLK inputs

7.4 Fuses

On UniBoard^2 a fuse is placed. The fuse is a 10A fast acting Littlefuse 154 Series type, part number 0453010. In Figure 7 the location of the fuse is shown.

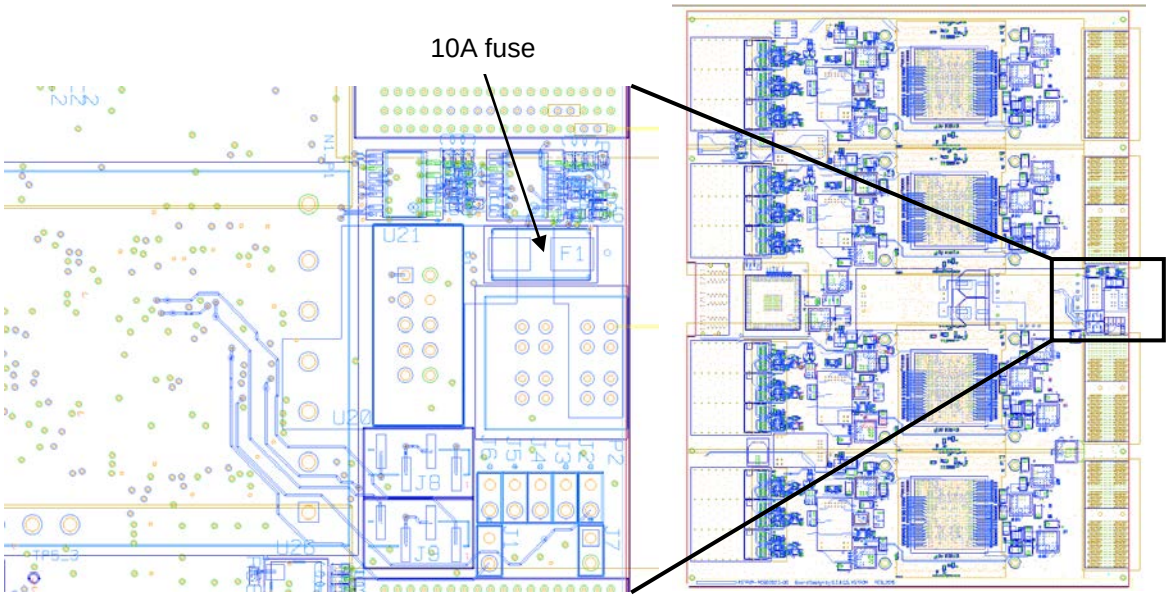

Figure 7 Fuse on UniBoard²

8 Default flash firmware image

In the flash a default image is programmed. When the board is powered up the QSFP LED's will be flashing red.

8.1 Board ID

Depending on the firmware an external ID can be used for example the Ethernet IP/MAC. In Figure 8 the location of the dip-switch is shown.

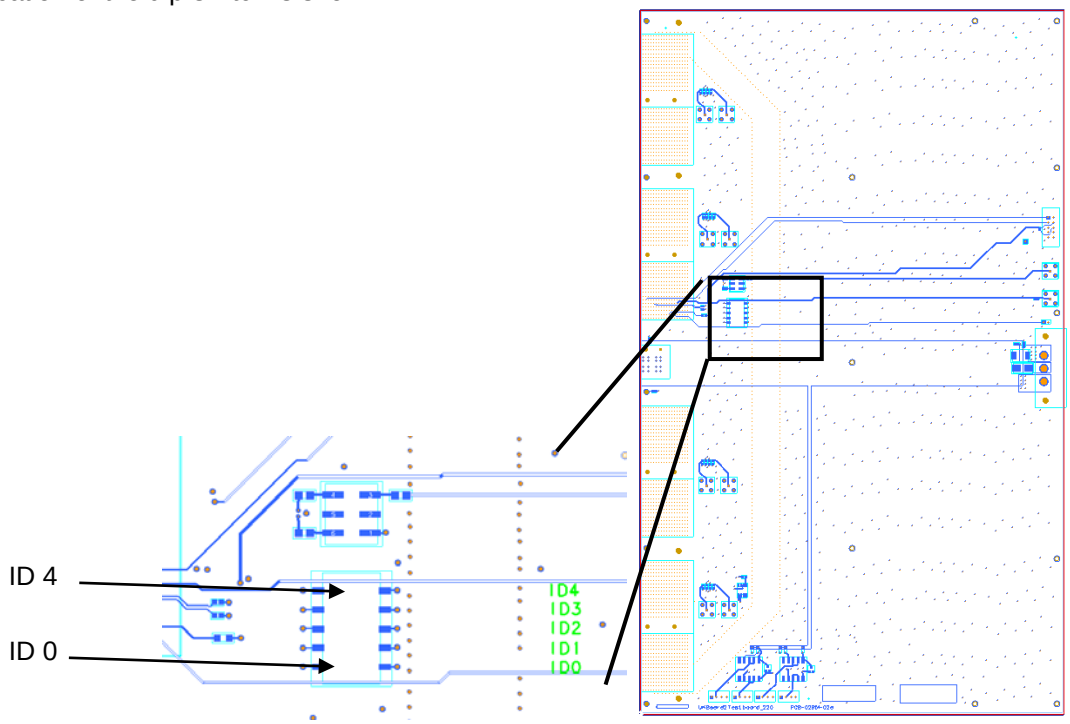

Figure 8 Location of Board ID

9 JUMPERS

9.1 JTAG jumpers

To use JTAG, Node 2 must be enabled, see section 9.3. In the firmware of the Lattice CPLD (U4) the JTAG jumpers are programmed as shown in Table 7.

Table 7 JTAG jumper functions

J6	J5	J4	J3	J2	Function
open	x	x	x	x	Scanbridge mode
placed	open	open	open	Open	All FPGAs in the loop
placed	x	x	x	placed	Skip node 0
placed	x	x	placed	x	Skip node 1
placed	x	placed	x	x	Skip node 2
placed	placed	X	x	x	Skip node 3

J8 and J9 must be placed to pin 1-2 for normal operation (to the backplane side of the board), by placing the jumpers to 3-4 the CPLD (U4) can be programmed. J1 and J7 are not used by the firmware in the Lattice device (U4). In Figure 9 the locations of the jumpers are shown.

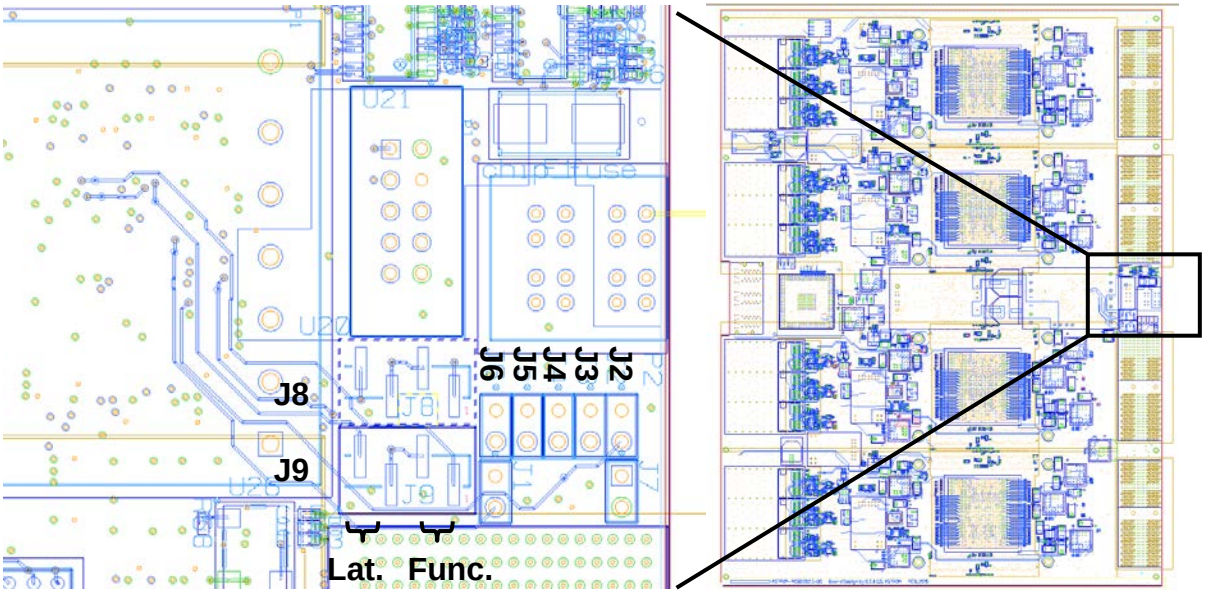

Figure 9 JTAG jumper locations

For programming the FPGAs with the Altera USBBlasterII the FPGAs can be placed in a single loop by placing only J6 (see Table 7). In Altera's Quartus II programming utility Node 0 is placed at location 1, Node 1 at location 2, Node 2 at location 3 and Node 3 at location 4.

9.2 Clock jumpers

9.2.1 System clock

With J12 1-2 the clock can be selected. By placing the jumper the Crystal Oscillator on UniBoard^2 is used. By removing the jumper the input from the backplane is used. In Figure 10 the location of the jumpers are shown.

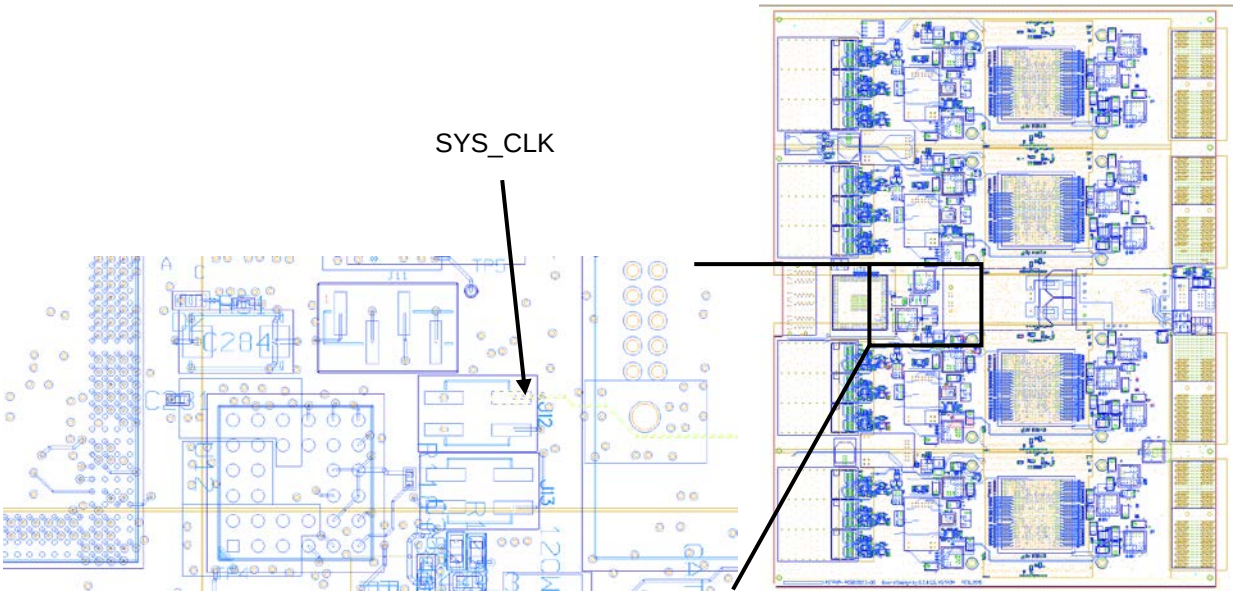

Figure 10 Location of clock selection jumpers

9.2.2 Transceiver clocks

To enable the transceiver clocks the jumpers J13 3-4 (SER_CLK_A) and J12 3-4 (SER_CLK_B) should be placed, see Figure 11 Location of Transceiver clock enable jumpers

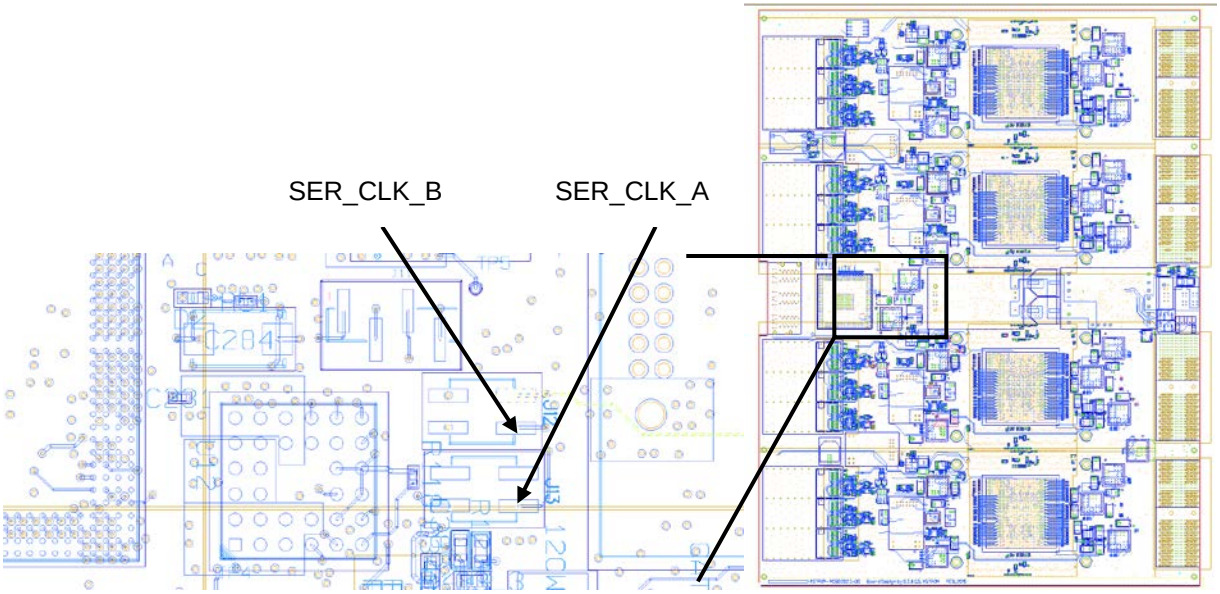

Figure 11 Location of Transceiver clock enable jumpers

9.3 Power supply jumpers

The power of every FPGA can be disabled when needed. For this J3_x is placed next to every FPGA, see Figure 12. By placing the jumper between 1-2 the FPGA are powered as normal, by placing the jumper between 3-4 the power of the FPGA is disabled.

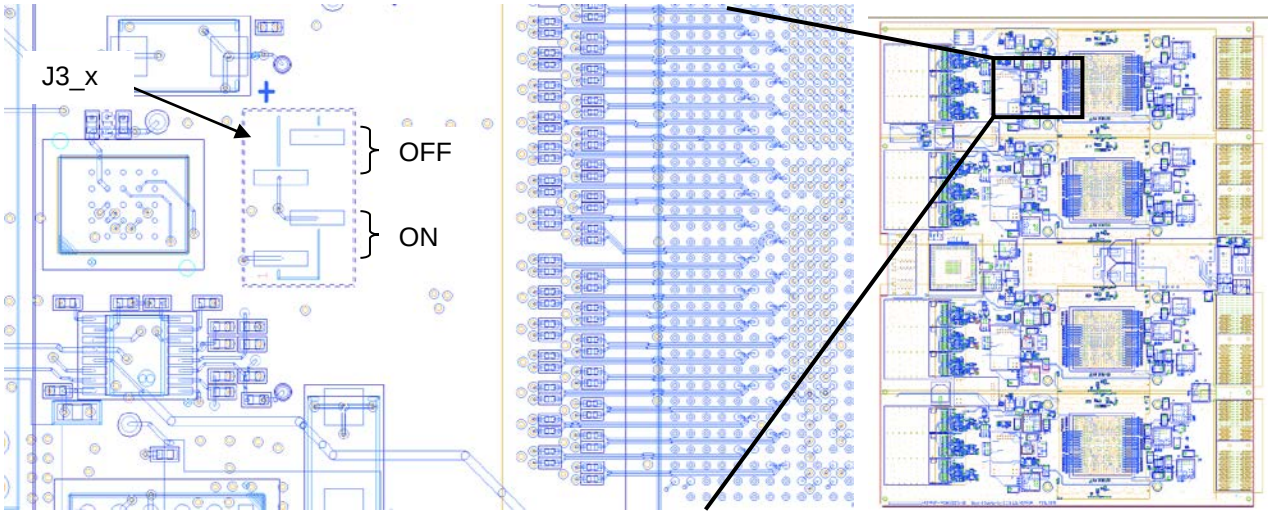

Figure 12 FPGA Power enable jumpers

10 LEDs

The power LED is integrated in the ON/OFF switch, the functions of the LED are shown in Table 8.

Table 8 Power LED

LED	State
Red	Power down
Green	Power on

On the QSFP cages light pipes are placed to show a LED per cage. The function of the LED is determined by the firmware. The function of the LED for the factory image is shown in Table 9

Table 9 QSFP Cage LED

LED	State
Red	UNB2 minimal
Green	Firmware dependent

11 On board connectors

On UniBoard² some debug connectors are placed on the board. In the following subsection these connectors are explained.

11.1 Ethernet switch readout

On UniBoard² a connector is placed for a RS232 terminal to readout the statistics of the Ethernet switch. In Figure 13 the pinning of the connector is shown.

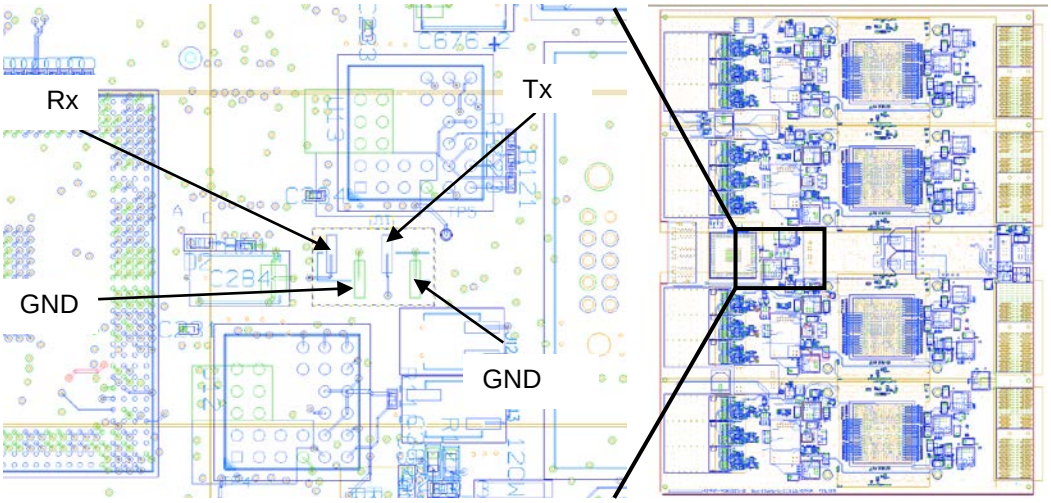

Figure 13 Switch Terminal Connector

For the communication to UniBoard^2 Realterm could be used. The COM port must be set to 8 data bits, 1 stop bit, no parity, 9600 baud and without flow control.

In the following subsections debug functions are described. The basic functions are described in [RD-5].

11.1.1 Version

With ‘v’ the version of the software and the chip can be readout. On the bottom of the version the mapping of the switch ports to FPGA and copper ports are shown, where “ll” stands for lower left RJ45 port, “ul” for upper left, “lr” for lower left and “ur” for the upper left port.
The result will look like:

```
UniBoard2 0.4
UniBoard2
Length Jumbo:  9600
Chip id: 273890e9

PRT0 PRT1 PRT2 PRT3 PRT4 PRT5 PRT6 PRT7 PRT8 PRT9 PRT10 PRT11 PRT12 PRT13
N0-0 N0-1 N1-0 N1-1 N2-0 N2-1 N3-0 N3-1 C ll C ul C lm  C um  C lr  C ur
```

11.1.2 Status

With ‘s’ the status of the switch can be readout. This will plot the status of the port and the number of transmitted and received octets since the last read out. The result will look like:

```
Port Status     RXOCT        TXOCT
 0   Port Up    0x00000000   0x00000000
 1   Port Down  0x00000000   0x00000000
 2   Port Up    0x00000000   0x00000000
 3   Port Down  0x00000000   0x00000000
 4   Port Up    0x00000000   0x00000000
 5   Port Down  0x00000000   0x00000000
 6   Port Up    0x00000000   0x00000000
 7   Port Down  0x00000000   0x00000000
 8   Port Down  0x00000000   0x00000000
 9   Port Up    0x00000000   0x00000000
10   Port Down  0x00000000   0x00000000
11   Port Down  0x00000000   0x00000000
12   Port Down  0x00000000   0x00000000
13   Port Down  0x00000000   0x00000000
```

11.1.3 Reboot

With ‘b’ the switch can be rebooted.

11.1.4 VLANs

VLANs can be enabled on the switch. By using command ‘L’ a list of the VLANs can be seen. By using command ‘ y’ VLANs can be set. The result of command ‘L’ after command ‘y’ is shown in Figure 14.

```
VLAN Table
Port Nr VLAN
 0       6
 1       5
 2       7
 3       5
 4       8
 5       5
 6       9
 7       5
 8       5
 9       5
10       6
11       7
12       8
13       9

VLAN P0 P1 P2 P3 P4 P5 P6 P7 P8 P9 P10 P11 P12 P13
 0
 1
 2
 3
 4
 5       X     X     X     X  X  X
 6    X                          X
 7          X                       X
 8                X                    X
 9                      X                    X
```

Figure 14 VLAN setting

11.2 Power readout

On Uniboard^2 digital power point of loads are placed. This will enable readout of the power consumption per regulator. This can be done by the FPGA, but for debugging an Ericsson controller and software can be used to readout and adjust the converters. For this a header is placed close to every FPGA, see Figure 15.

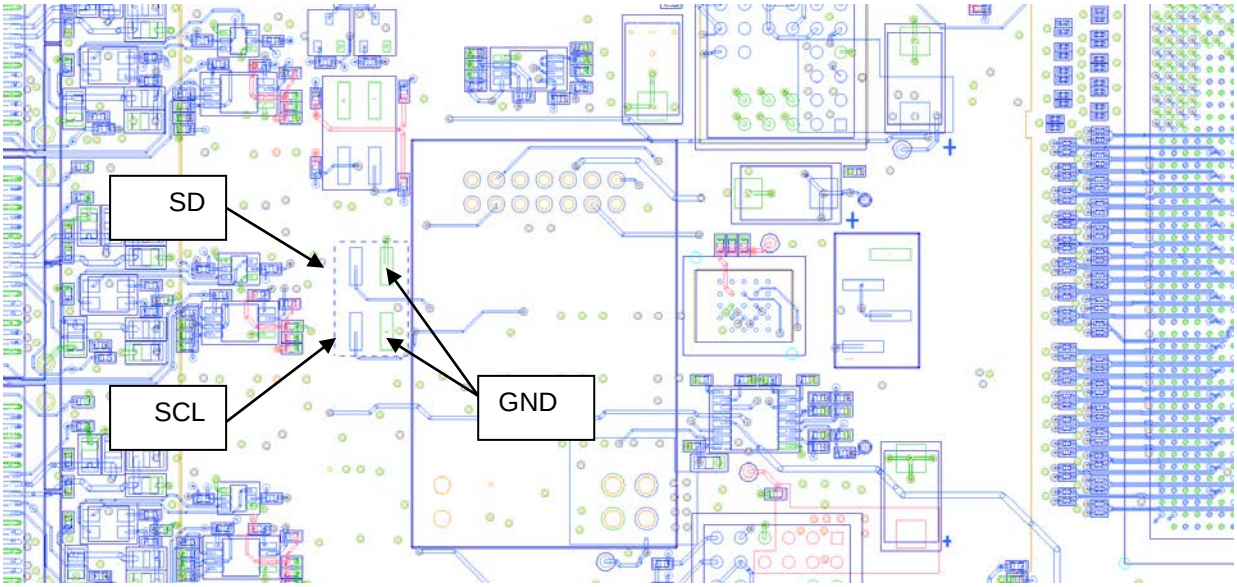

Figure 15 POL readout connector

The input DC/DC-converter and the central point of loads can be read out with an external controller as well. In Figure 16 the location of the connector is shown. Before the power can be readout J15 has to be placed.

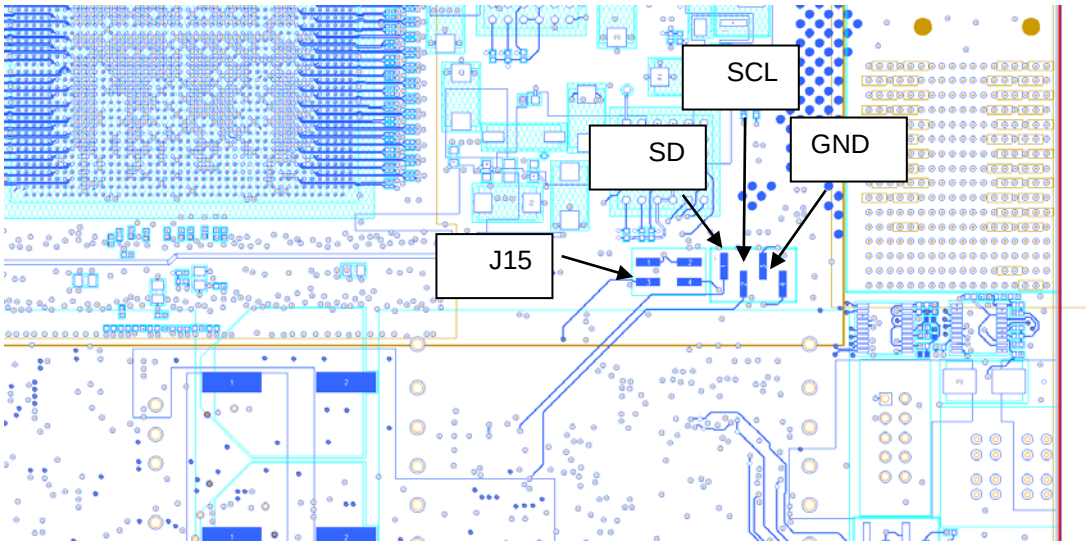

Figure 16 Central Power / POL readout connector

12 Liquid cooling

On UniBoard² liquid cooling is used. Two dedicated water blocks are placed on UniBoard² to cool the FPGAs. On the backside of the UniBoard² housing two quick release couplings are placed to connect the Swiftech MCR-X20 Heat Exchanger. According to the manual of the heat exchanger the orientation of the heat exchanger is important to keep the coolant circulating. In Figure 17 the options are shown.

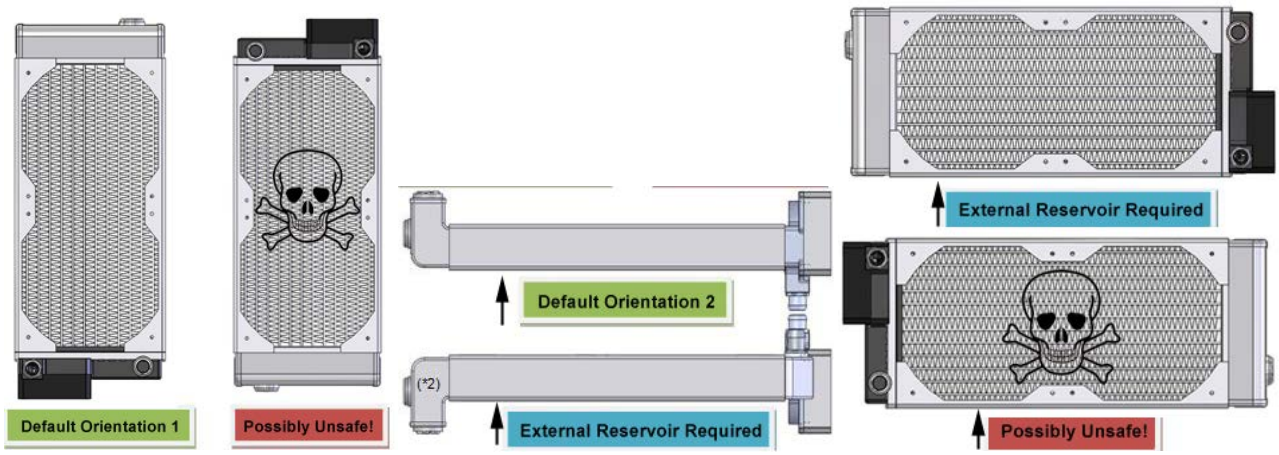

Figure 17 Orientation of the heat exchanger

A manual of the heat exchanger can be found at:
http://www.swiftech.org/Installation_guides/installation_guide-MCRX20-Drive-R3-EN.pdf

The UniBoard²s are supplied with the liquid system filled-up. However after some time it might be needed to fill up the system. In Figure 18 the filling is shown. It is best to have the pump running while filling up. For UniBoard² Aquatuning AT-Protect-UV Crystal Blue is used.

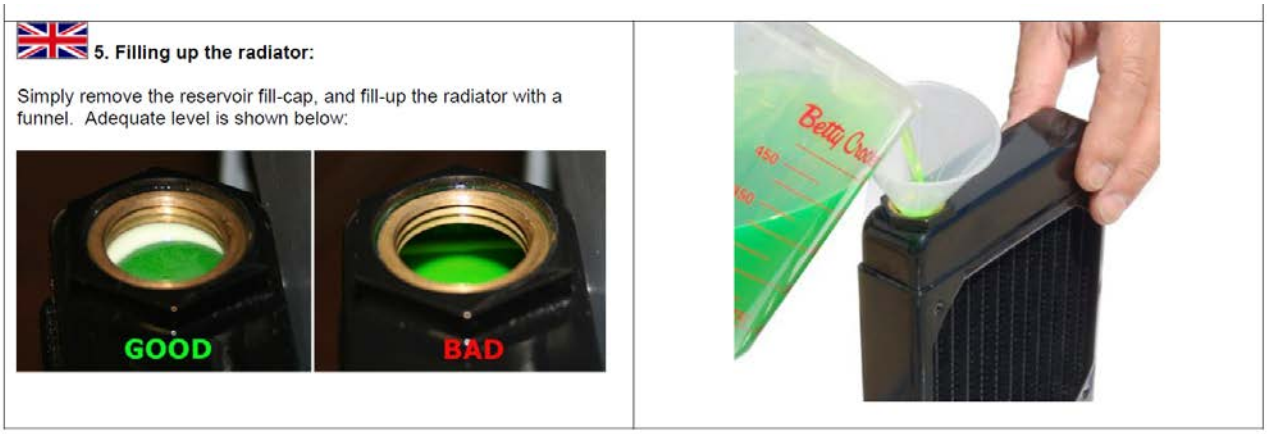

Figure 18 Filling-up the liquid system

13 Instrument markings

The instruction documentation symbol. The product is marked with this symbol when it is necessary for the user to refer to the instructions in the documentation.

This symbol indicates separate collection for electrical and electronic equipment, mandated under EU law as of August 13, 2005. All electrical and electronic equipment are required to be separated from normal waste for disposal (Reference WEEE Directive, 2002/96/EC.

The CE mark is a registered trademark of the European Community. (If accompanied by a year, it is when the design was proven.)

When optical transceivers are used, take care of (invisible) LASER Radiation. Do not stare into beam of the cable or optical transceiver or view directly with optical instruments